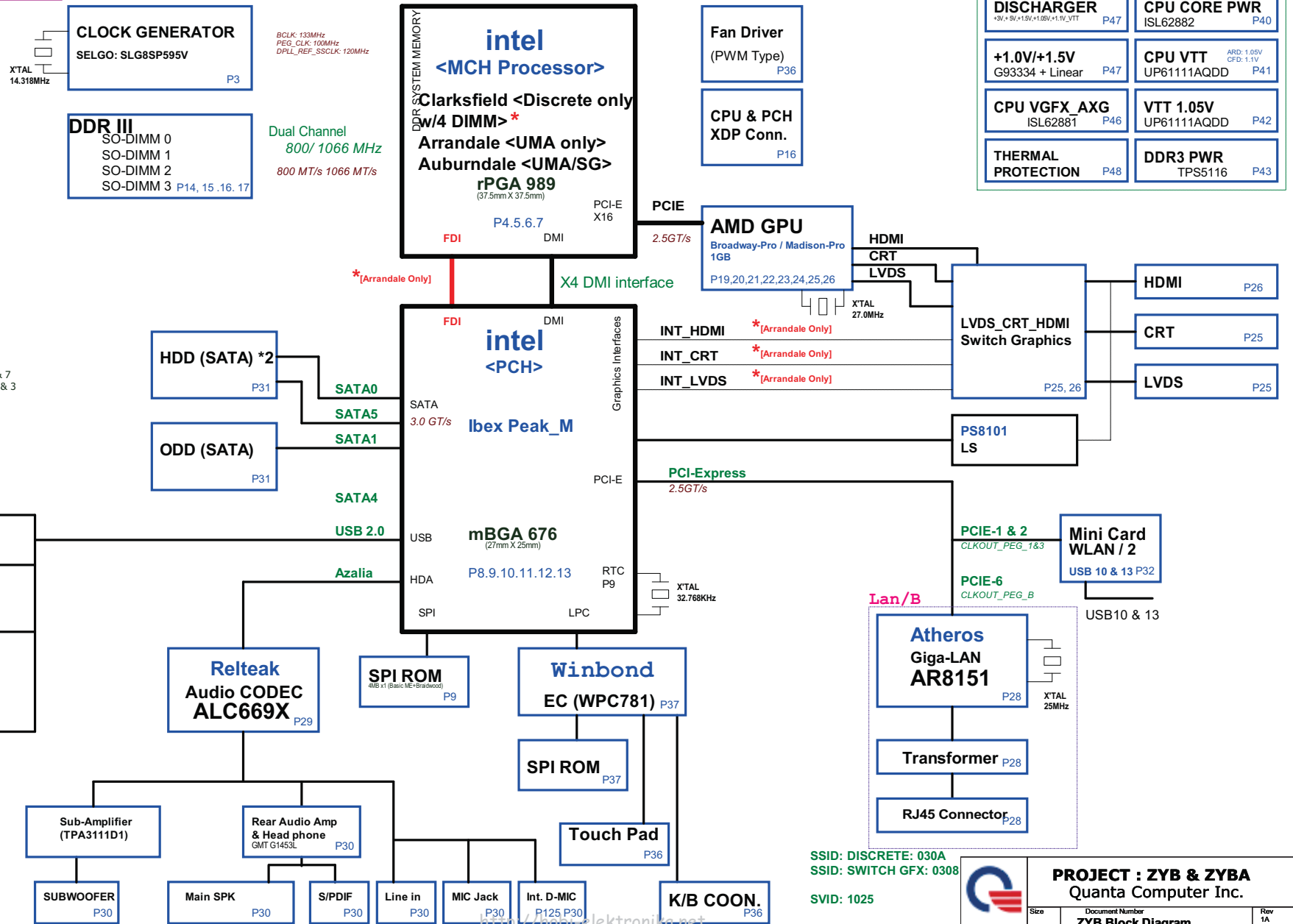
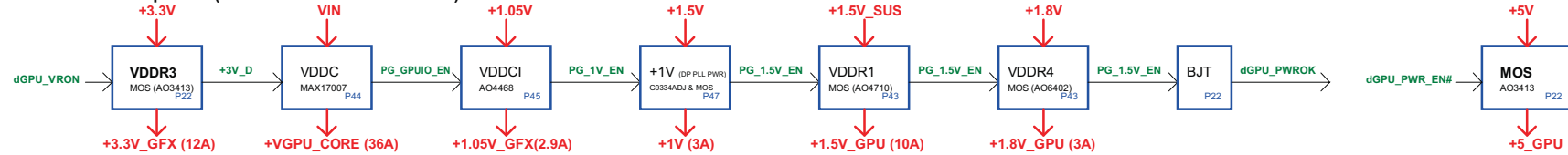


# ZYB & ZYBA SYSTEM BLOCK DIAGRAM

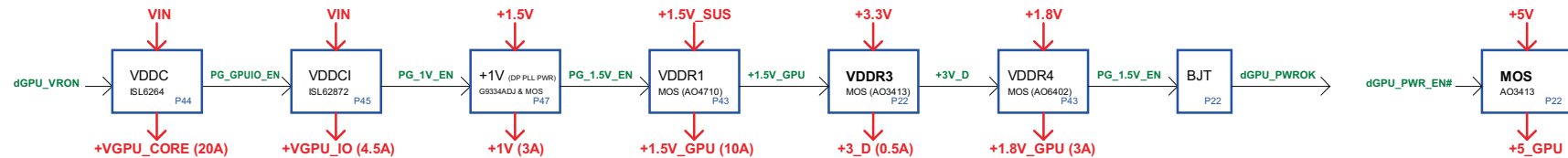
A@ --> Arrandale use  
E@ --> Discrete use  
SW@ --> Switch use  
IV@ --> UMA use



## GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



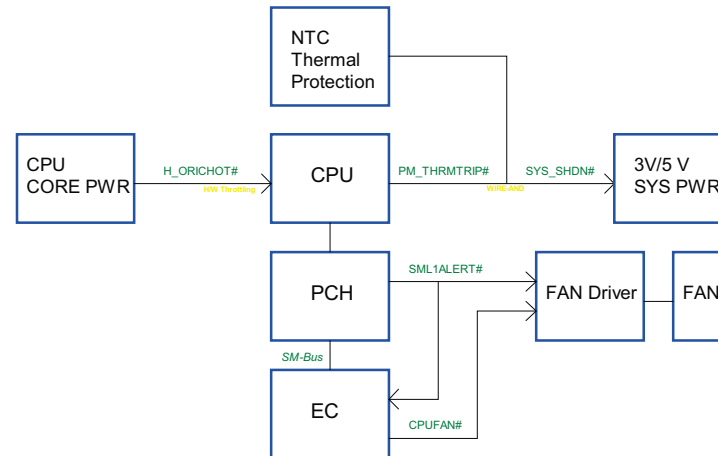
## GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

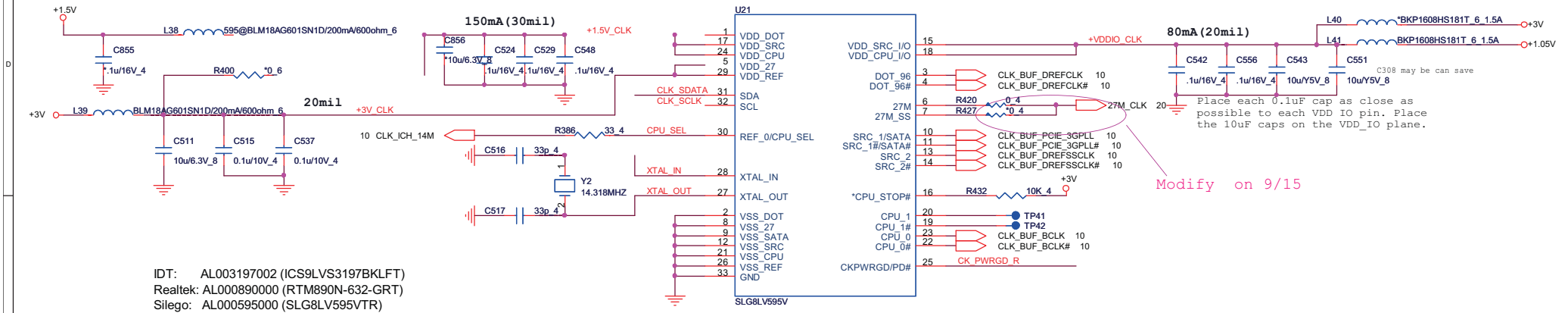


## Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5V_SUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+VGPUCORE	+0.9V~+1.1V	GPU CORE POWER	dGPU_VRON	Discrete enable
+1.05V_GFX	+0.9V~+1.1V	GPU I/O POWER	dGPU_VRON	Discrete enable
+1.5V_GFX	+1.5V	VRAM CORE POWER	dGPU_VRON	Discrete enable
+1.8V_VGA	+1.8V	LVDS/PLL POWER	dGPU_VRON	Discrete enable
+3.3V_GFX	+3.3V	PEG/HDMI/CRT POWER	dGPU_VRON	Discrete enable

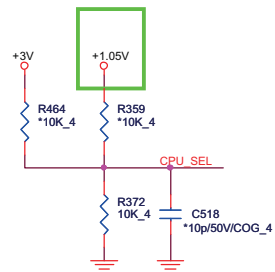
## Thermal Follow Chart





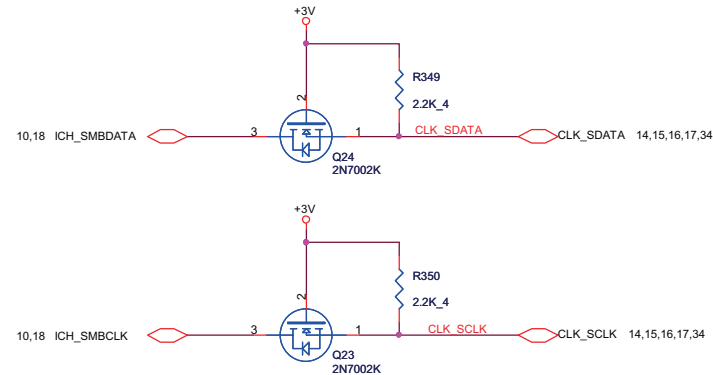
## CPU\_CLK select

Modify on C test

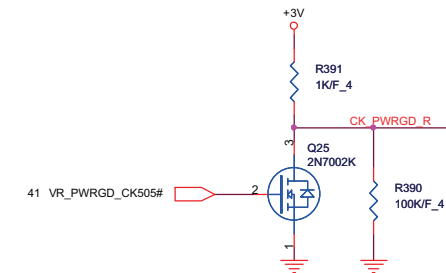


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

## SMBus



## CLK Enable

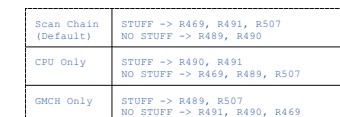


**PROJECT : ZYB & ZYBA**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>Clock Generator</b>	1A
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## JTAG MAPPING



+1.5V\_CPU/VDDQ

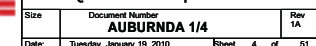
R216  
1.1K F4

PM RAM PWIRGO

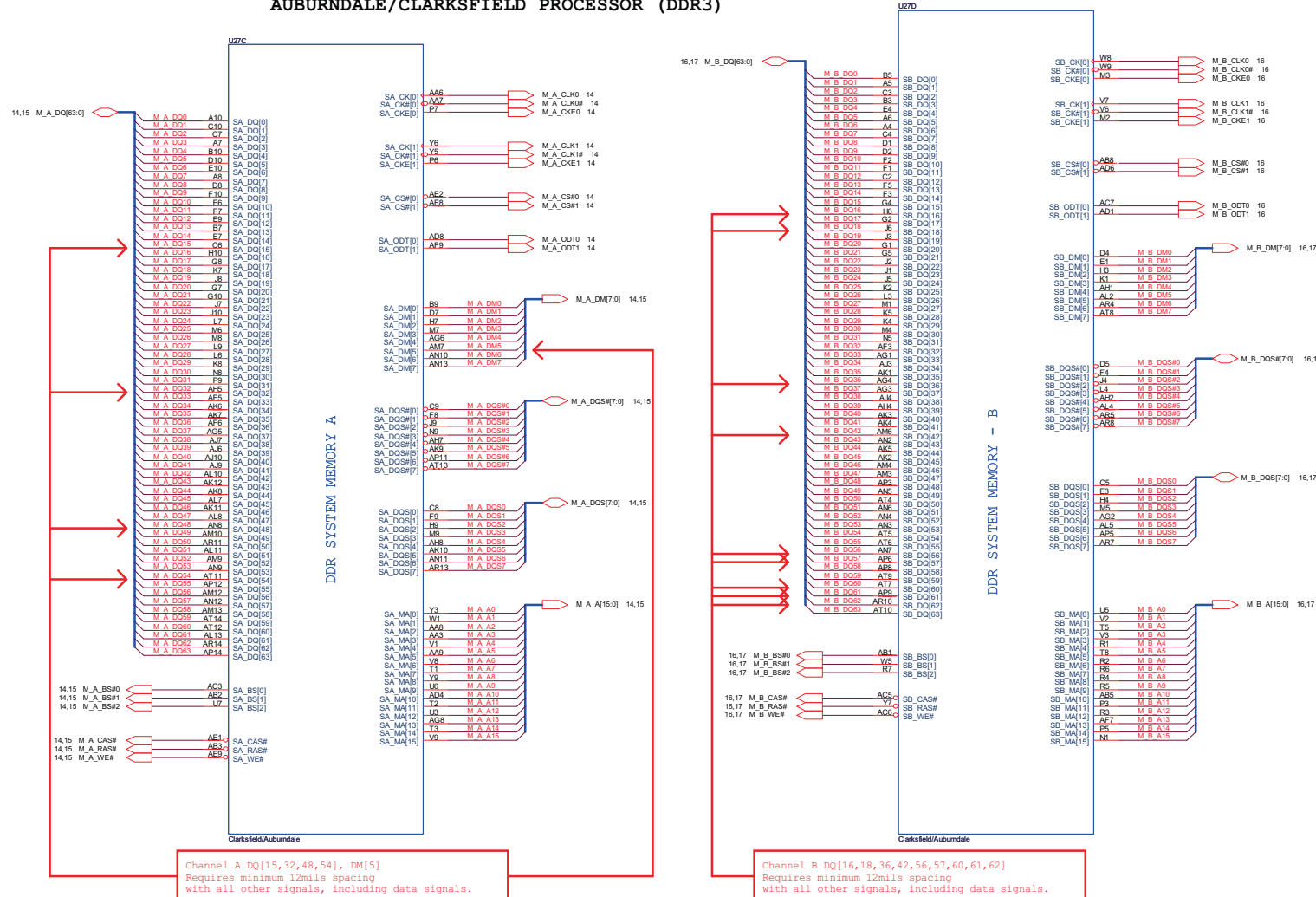
R213  
3K F4

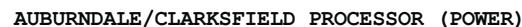
Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.

Note: CBR uses a 3.3V (always ON) rail with 2K and 1K combination.

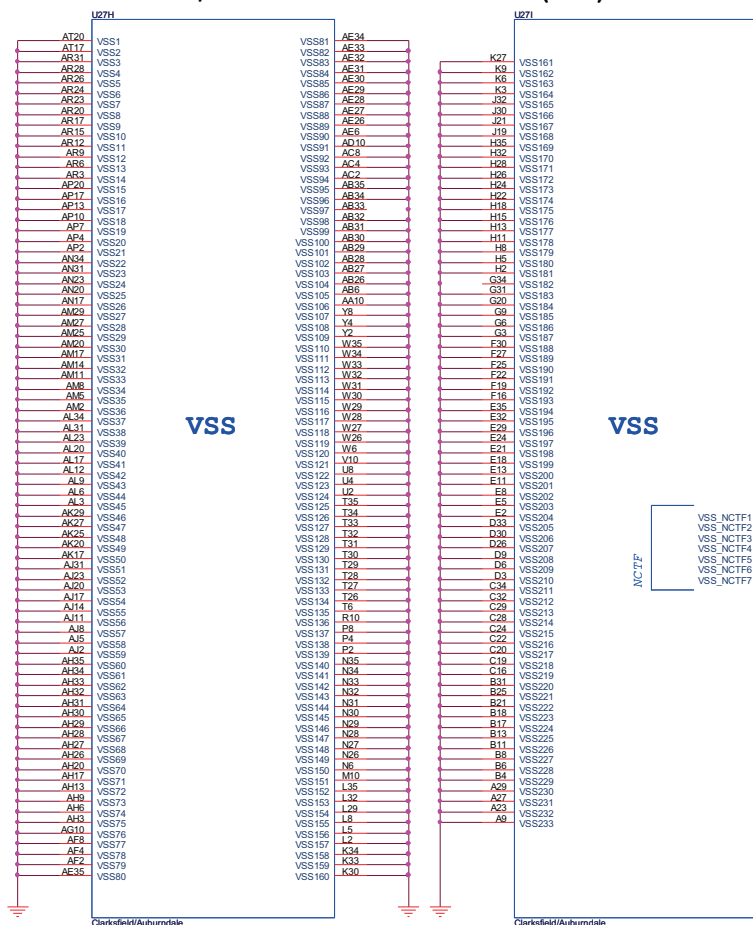


## AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

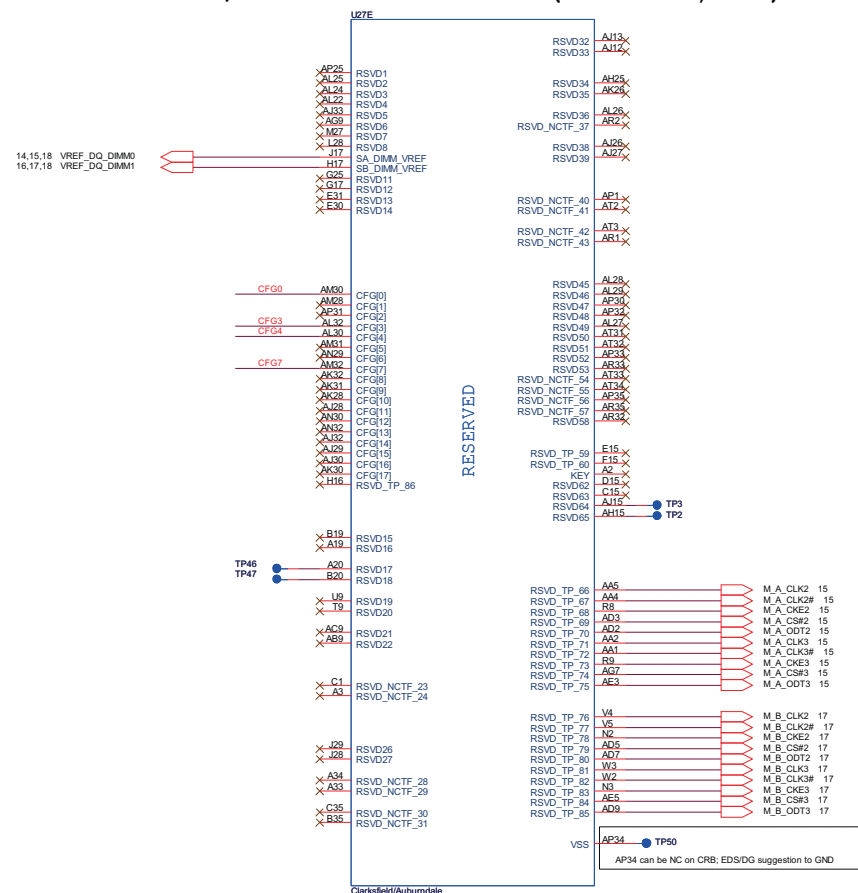




AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

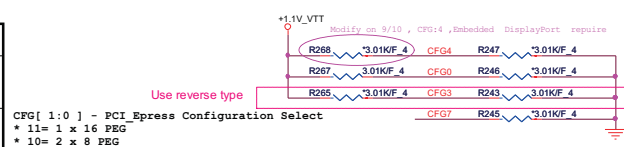


## AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)



## Processor Strapping

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed



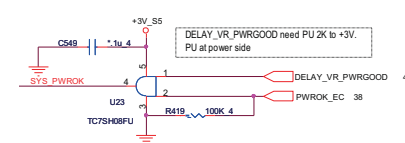
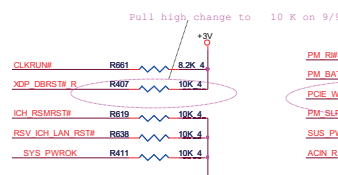
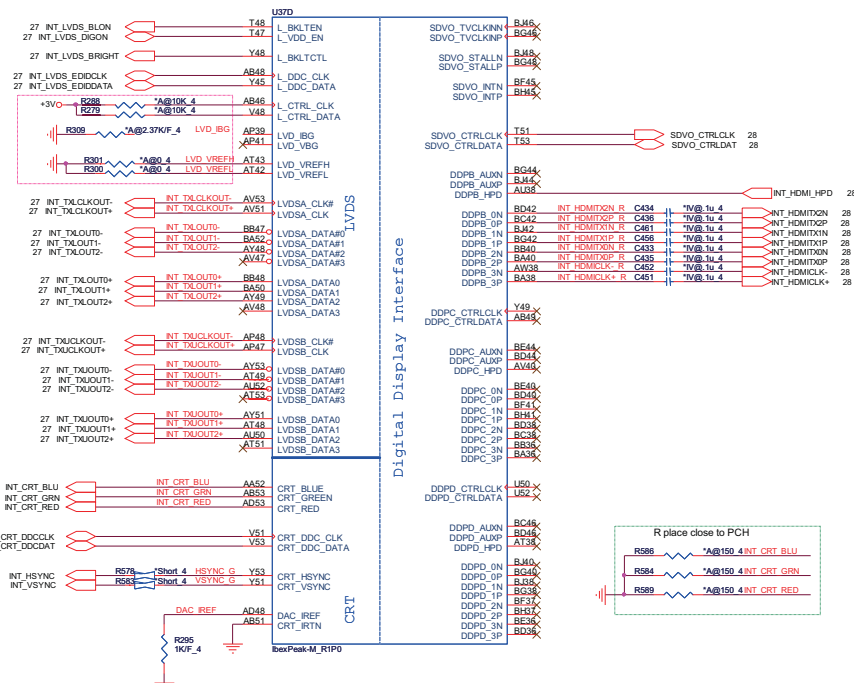
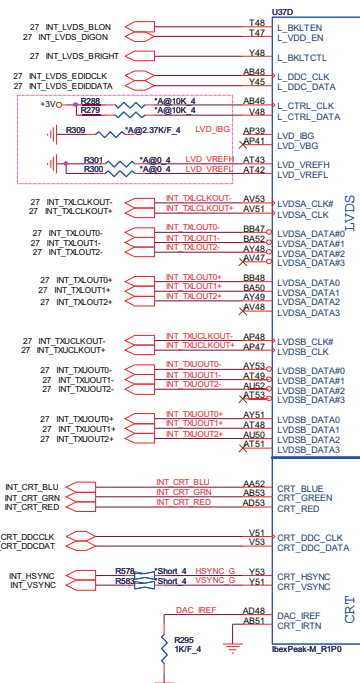
The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed. (ES1 only)



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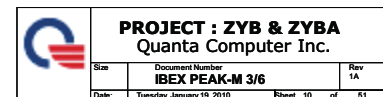
Size	Document Number <b>AUBURND 4/4</b>	Rev 1A
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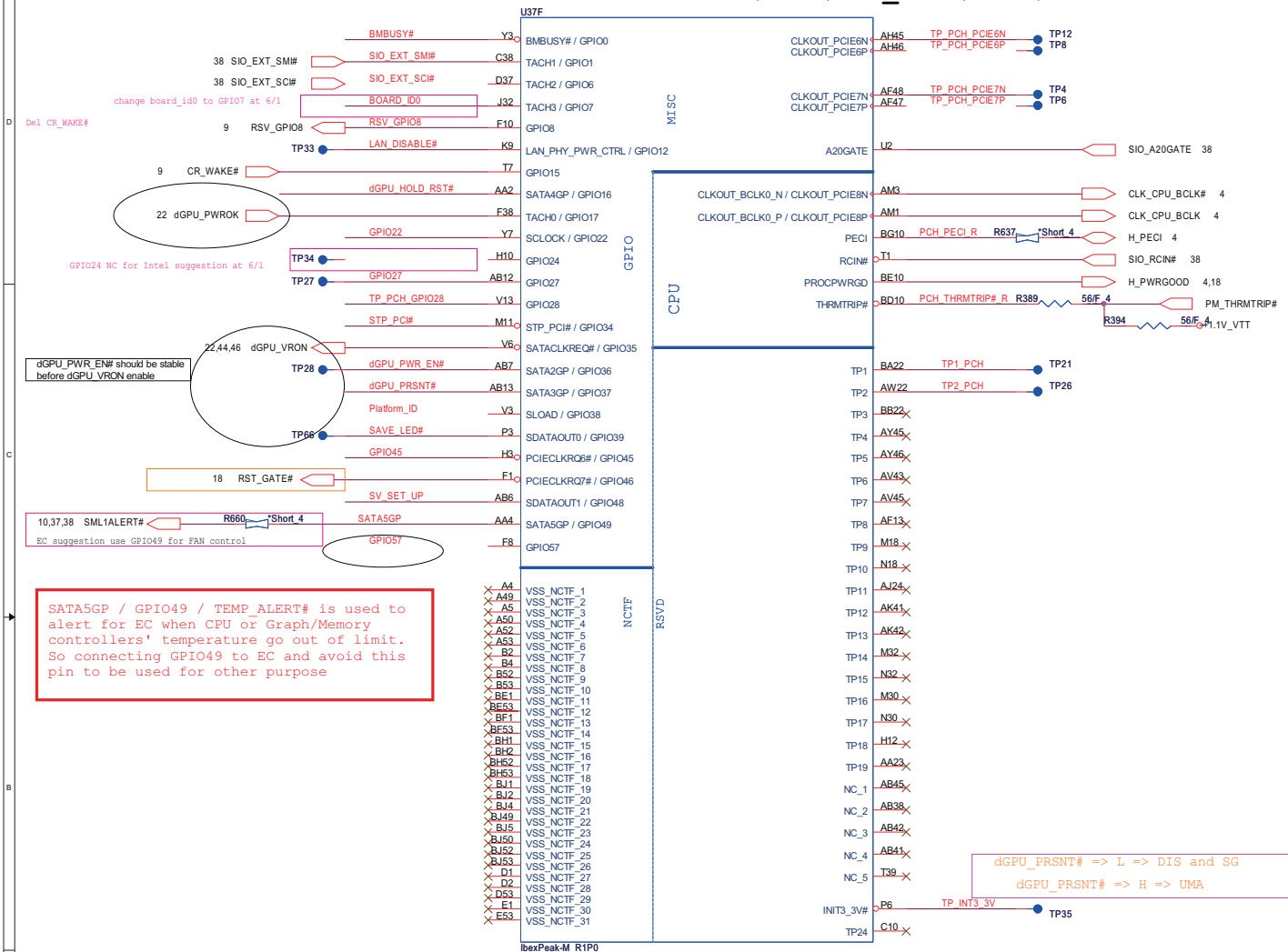






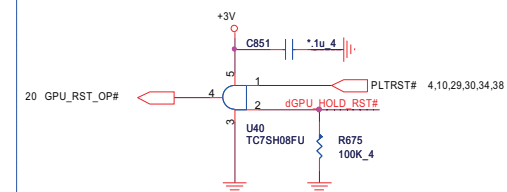


# IBEX PEAK-M (GPIO,VSS\_NCTF,RSVD)

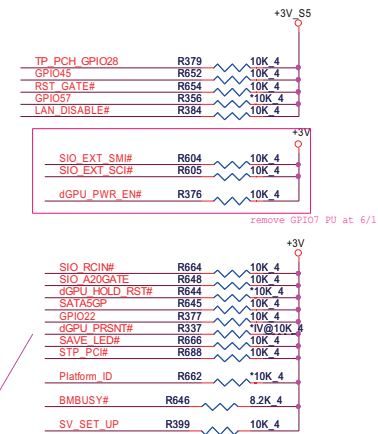


## GPU RST#

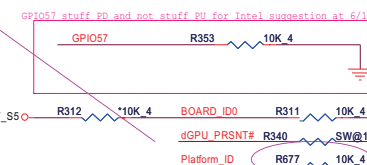
11



## GPIO Pull-up/Pull-down



SV\_SET\_UP 1-X High = Strong (Default)



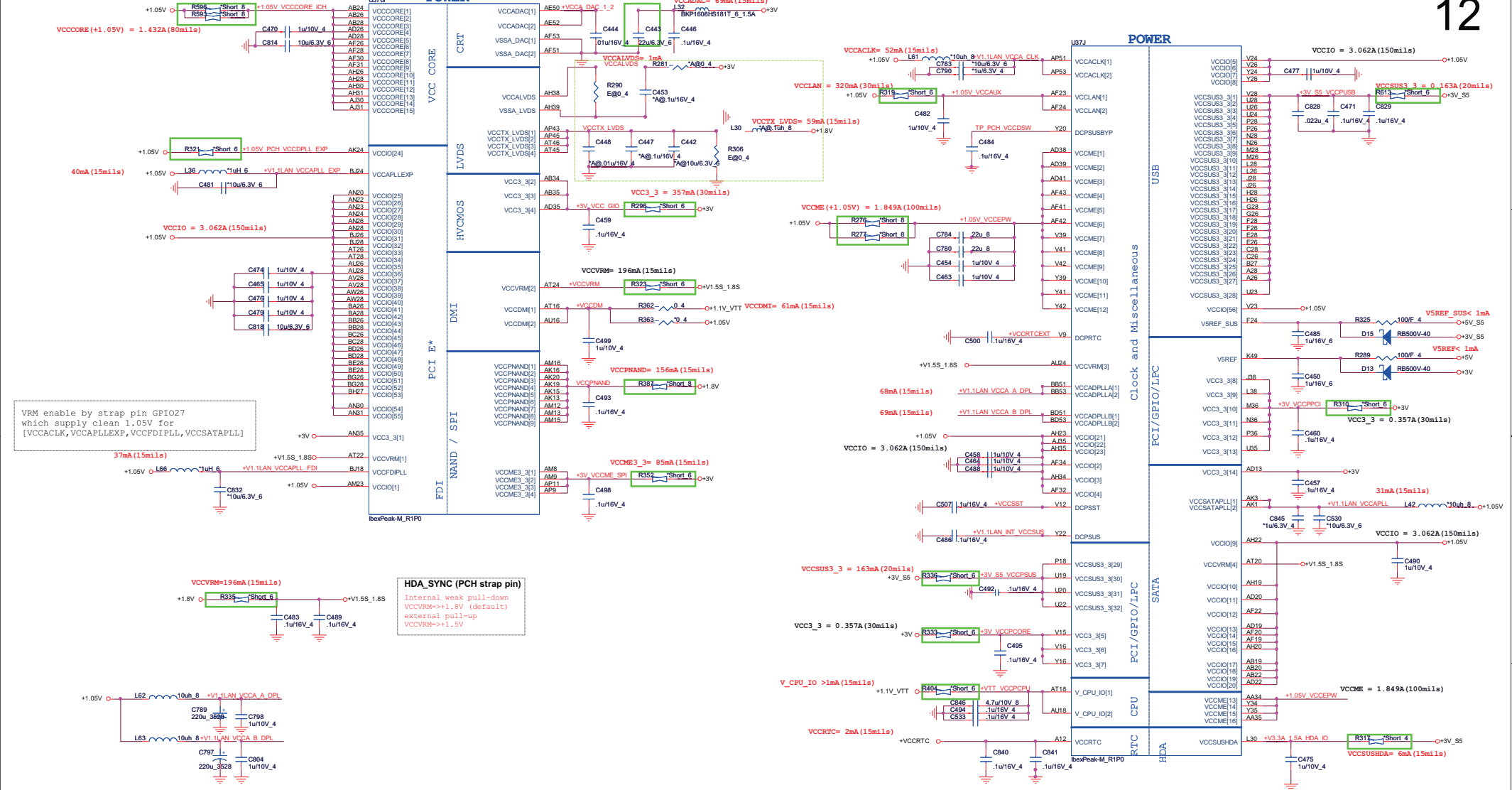
Integrated Clock Chip Enable	
BOARD_ID0	High = Discrete Low = SW
RSV_GPIO8	High = Disable Low = Enable



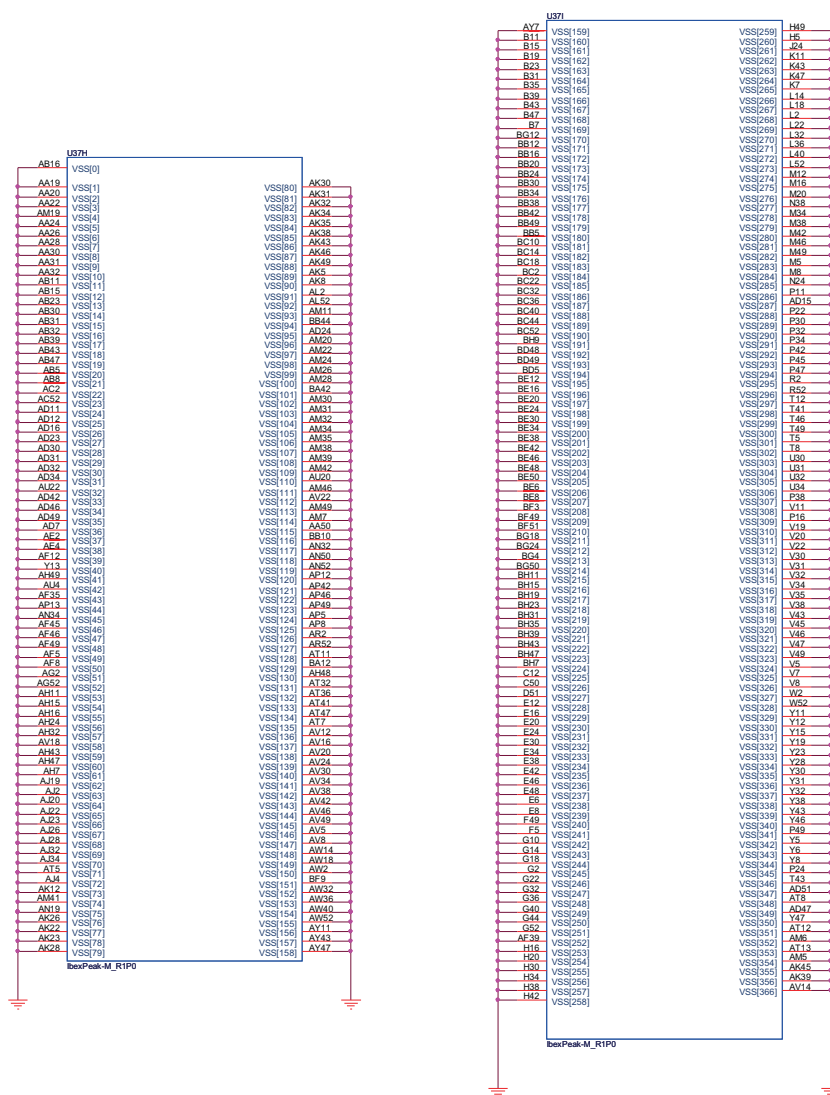
**PROJECT : ZYB & ZYBA**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>IBEX PEAK-M 4/6</b>	1A
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## IBEX PEAK-M (POWER)

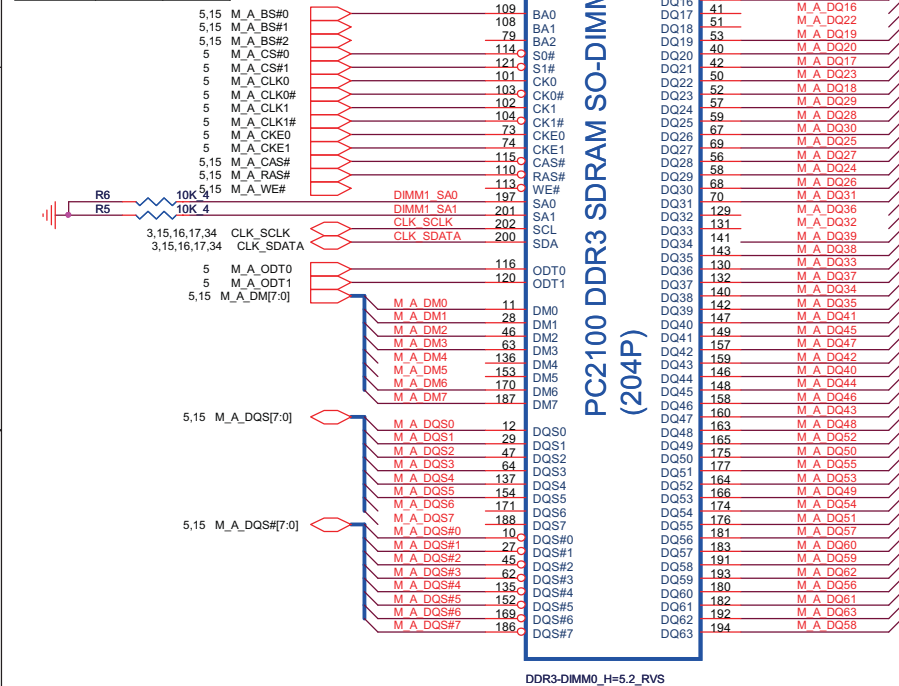


## IBEX PEAK-M (GND)



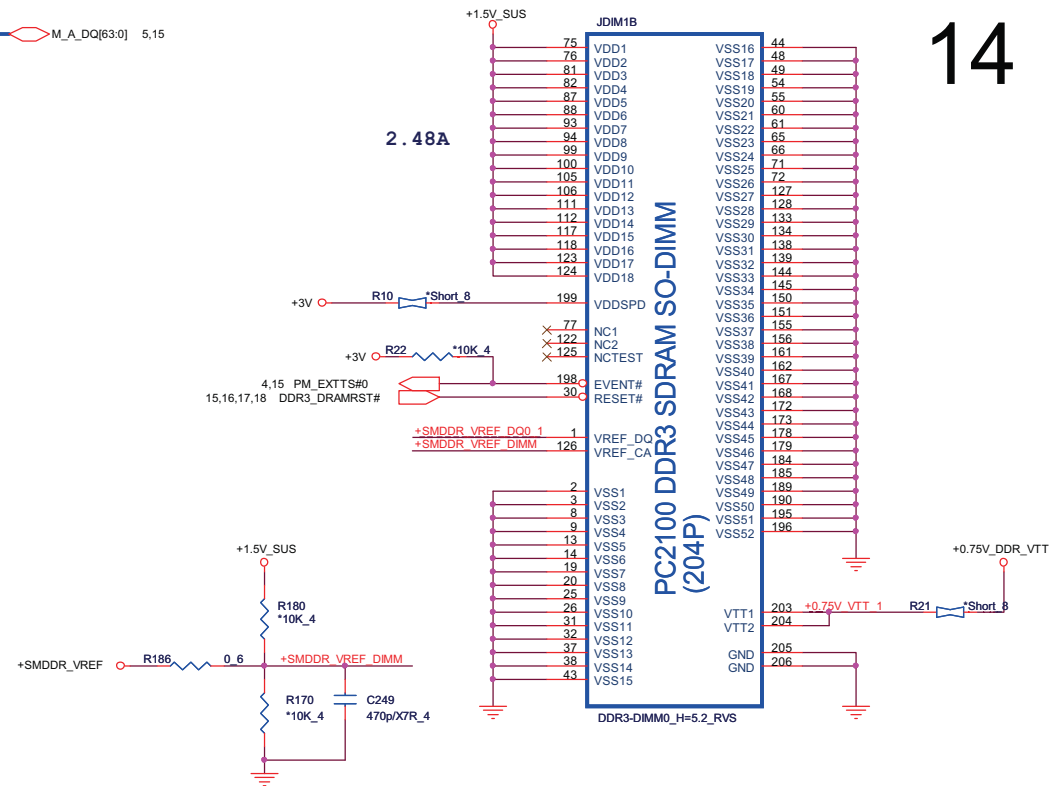
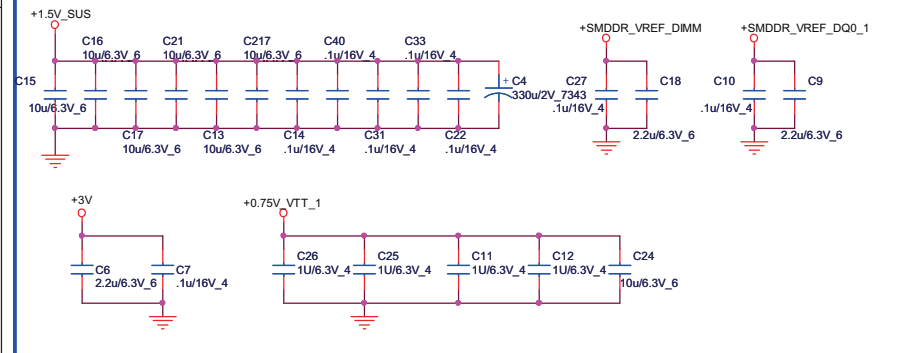
## DDR\_RVS (DDR)

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	1
CHB1	1	0

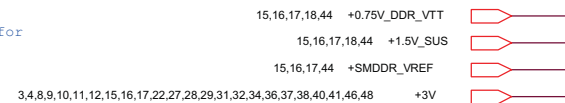
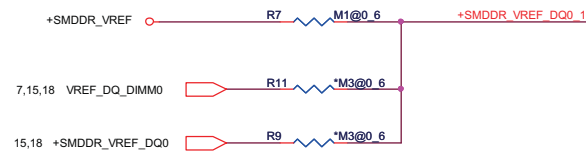


DDR3-DIMM0\_H=5.2\_RVS

**Place these Caps near So-Dimm0.**



DM signals are not present on Clarksfield processor. All DM signals can be left as No Connect on Clarksfield and connected directly to GND on SO-DIMM side for Clarksfield only designs.



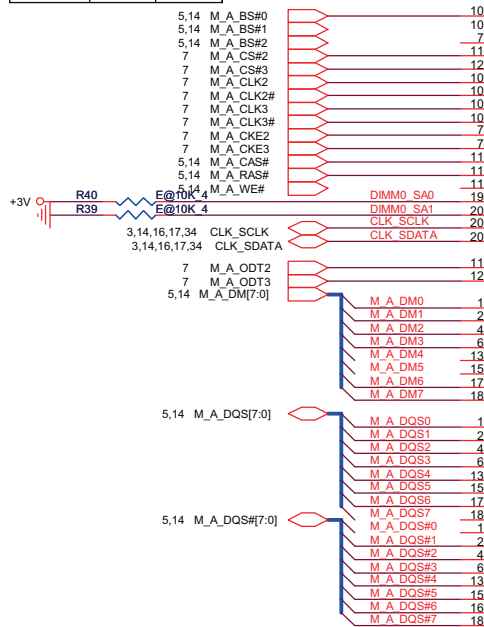
**PROJECT : ZYB & ZYBA**  
Quanta Computer Inc.

Size	Document Number <b>DDR3 SO-DIMM-0</b>	Rev 1A
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# DDR\_RVS (DDR)

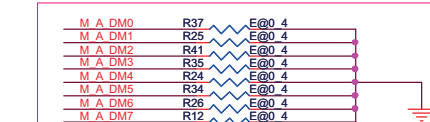
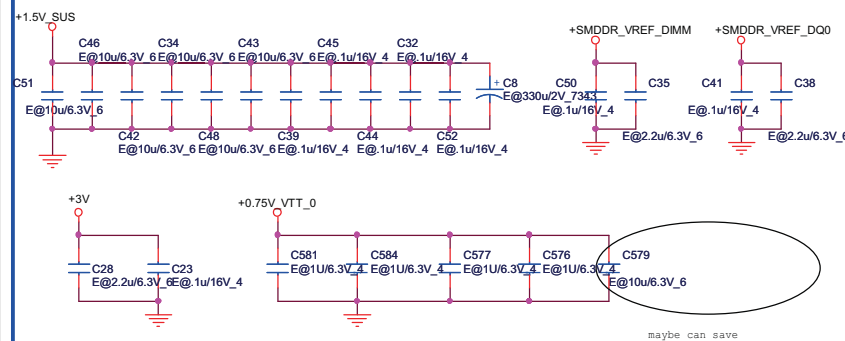
	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	1
CHB1	1	0



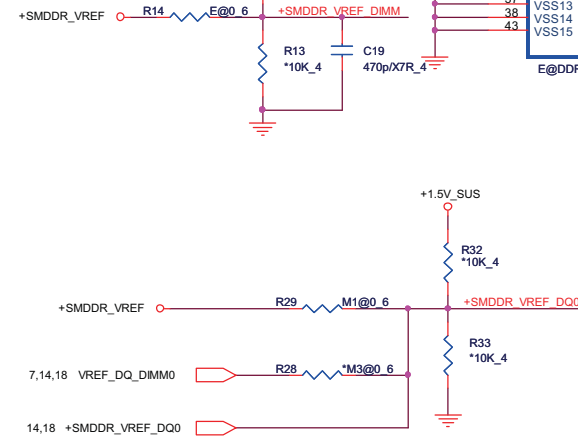
PC2100 DDR3 SDRAM SO-DIMM (204P)

E@DDR3-DIMM0\_H=9.2\_RVS

Place these Caps near So-Dimm0.



http://hobi-elektronika.net



Close to SO-DIMM

PC2100 DDR3 SDRAM SO-DIMM (204P)

E@DDR3-DIMM0\_H=9.2\_RVS



**PROJECT : ZYB & ZYBA**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>DDR3 SO-DIMM-0</b>	<b>1A</b>
Date:	Tuesday, January 19, 2010	Sheet 15 of 51



# DDR\_RVS (DDR)

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1

5,17	M_B_BS#0
5,17	M_B_BS#1
5,17	M_B_CS#0
5	M_B_CS#1
5	M_B_CLK0
5	M_B_CLK0#
5	M_B_CLK1
5	M_B_CLK1#
5	M_B_CKE0
5	M_B_CKE1
5,17	M_B_CAS#
5,17	M_B_RAS#
5,17	M_B_WE#

3,14,15,17,34	CLK_SCLK
3,14,15,17,34	CLK_SDAT
5	M_B_ODT0
5	M_B_ODT1
5,17	M_B_DM[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

5,17	M_B_DQS[7:0]
5,17	M_B_DQS#7[7:0]

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

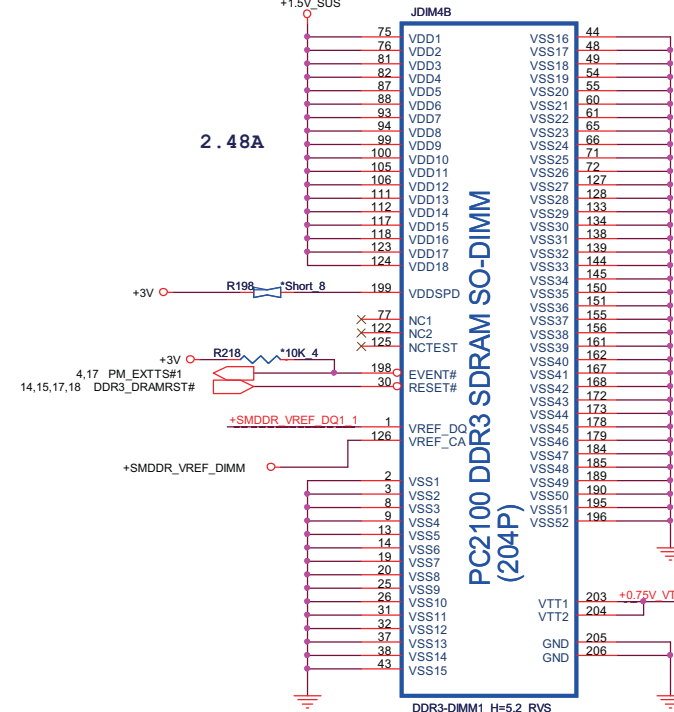
M_B_A0	98
M_B_A1	97
M_B_A2	96
M_B_A3	95
M_B_A4	94
M_B_A5	91
M_B_A6	90
M_B_A7	86
M_B_A8	89
M_B_A9	85
M_B_A10	107
M_B_A11	84
M_B_A12	83
M_B_A13	119
M_B_A14	80
M_B_A15	78

## PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1\_H=5.2\_RVS

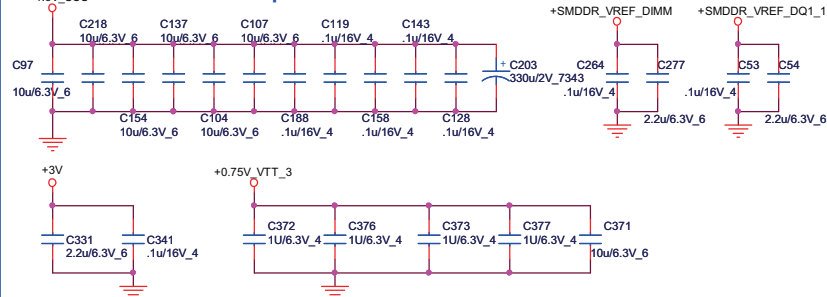
DO0	5	M_B_DQ05
DQ1	7	M_B_DQ1
DQ2	15	M_B_DQ3
DQ3	17	M_B_DQ7
DQ4	4	M_B_DQ0
DQ5	6	M_B_DQ6
DQ6	16	M_B_DQ2
DQ7	18	M_B_DQ4
DQ8	21	M_B_DQ12
DQ9	23	M_B_DQ13
DQ10	33	M_B_DQ14
DQ11	35	M_B_DQ15
DQ12	22	M_B_DQ9
DQ13	24	M_B_DQ8
DQ14	34	M_B_DQ10
DQ15	36	M_B_DQ11
DQ16	39	M_B_DQ16
DQ17	41	M_B_DQ20
DQ18	51	M_B_DQ22
DQ19	53	M_B_DQ23
DQ20	40	M_B_DQ17
DQ21	42	M_B_DQ21
DQ22	50	M_B_DQ19
DQ23	52	M_B_DQ18
DQ24	57	M_B_DQ24
DQ25	59	M_B_DQ28
DQ26	67	M_B_DQ26
DQ27	69	M_B_DQ30
DQ28	56	M_B_DQ29
DQ29	58	M_B_DQ25
DQ30	68	M_B_DQ27
DQ31	70	M_B_DQ31
DQ32	129	M_B_DQ32
DQ33	131	M_B_DQ33
DQ34	141	M_B_DQ34
DQ35	143	M_B_DQ39
DQ36	130	M_B_DQ35
DQ37	132	M_B_DQ37
DQ38	140	M_B_DQ35
DQ39	142	M_B_DQ38
DQ40	147	M_B_DQ45
DQ41	149	M_B_DQ40
DQ42	157	M_B_DQ43
DQ43	159	M_B_DQ47
DQ44	146	M_B_DQ41
DQ45	148	M_B_DQ44
DQ46	158	M_B_DQ46
DQ47	160	M_B_DQ42
DQ48	163	M_B_DQ48
DQ49	165	M_B_DQ53
DQ50	175	M_B_DQ50
DQ51	177	M_B_DQ55
DQ52	164	M_B_DQ52
DQ53	166	M_B_DQ49
DQ54	174	M_B_DQ54
DQ55	176	M_B_DQ51
DQ56	181	M_B_DQ57
DQ57	183	M_B_DQ60
DQ58	191	M_B_DQ59
DQ59	193	M_B_DQ63
DQ60	180	M_B_DQ56
DQ61	182	M_B_DQ58
DQ62	192	M_B_DQ62
DQ63	194	M_B_DQ61

M\_B\_DQ[63:0] 5,17



16

## Place these Caps near So-Dimm1.



<http://hobi-elektronika.net>

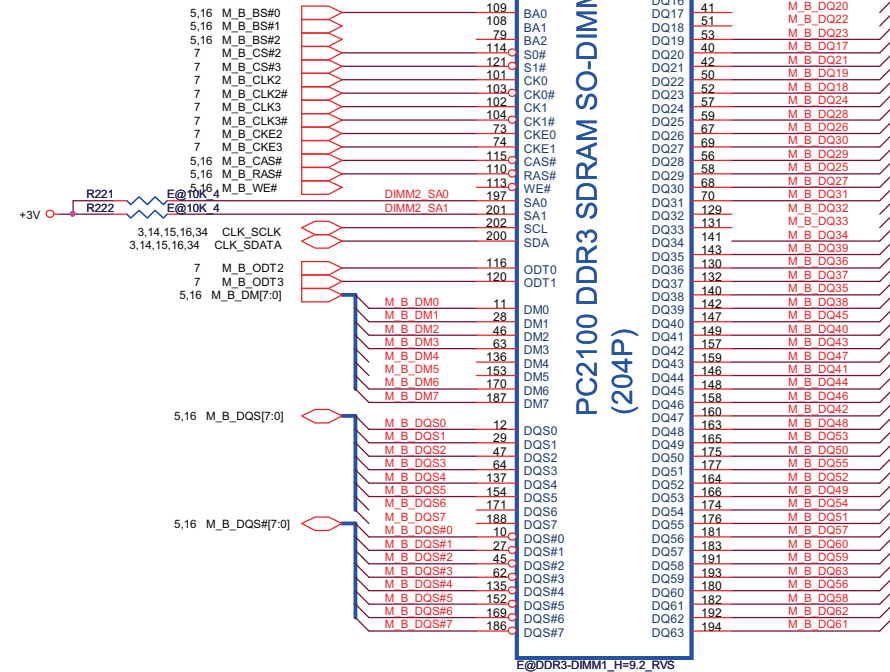


**PROJECT : ZYB & ZYBA**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	DDR3 SO-DIMM-1	1A
Date:	Tuesday, January 19, 2010	Sheet 16 of 51

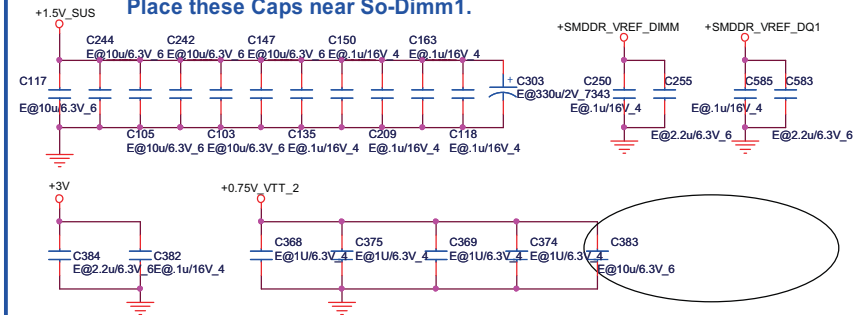
# DDR\_RVS (DDR)

	SA1	SA0
CHA0	0	0
CHA1	0	1
CHB0	1	0
CHB1	1	1



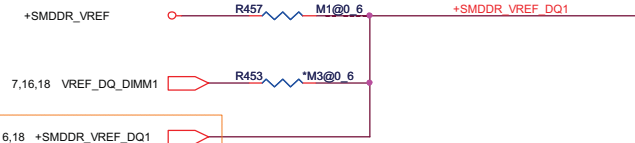
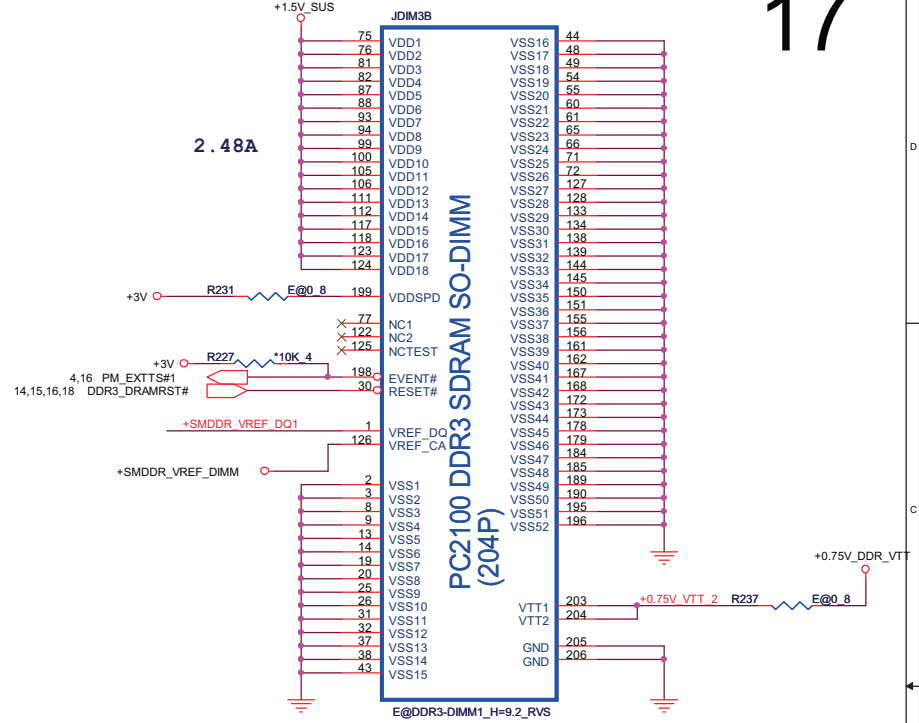
E@DDR3-DIMM1\_H=9\_2\_RVS

## Place these Caps near So-Dimm1.



maybe can save

M\_B\_DQ[63:0] 5,16



Close to SO-DIMM

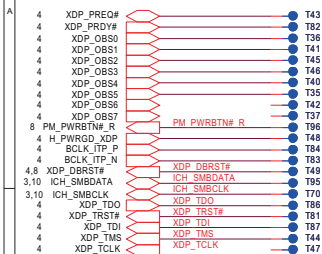


<http://hobi-elektronika.net>

**PROJECT : ZYB & ZYBA**  
Quanta Computer Inc.

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date:	Tuesday, January 19, 2010	Sheet 17 of 51

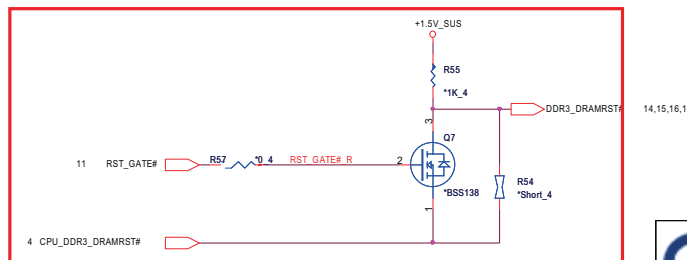
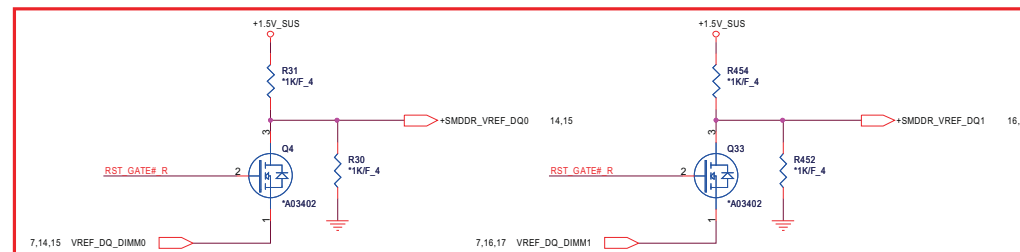
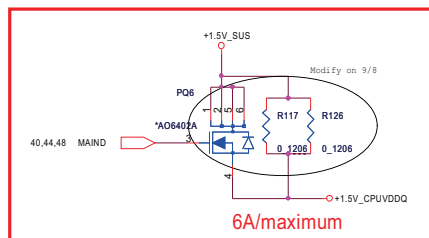
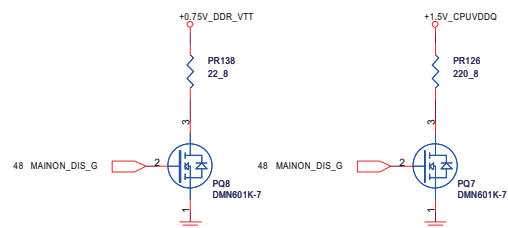
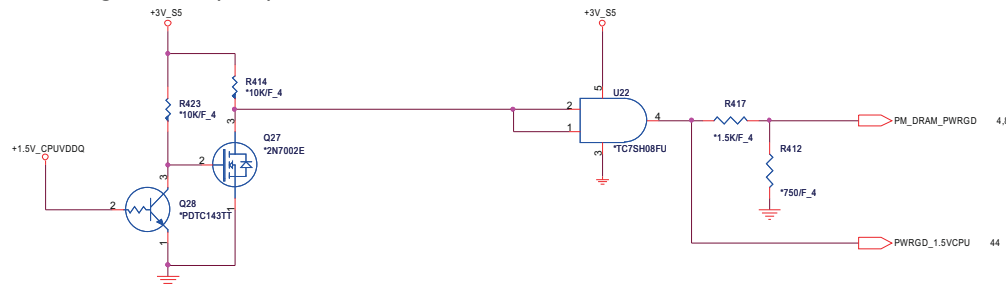
# Del CPU XDP Connector

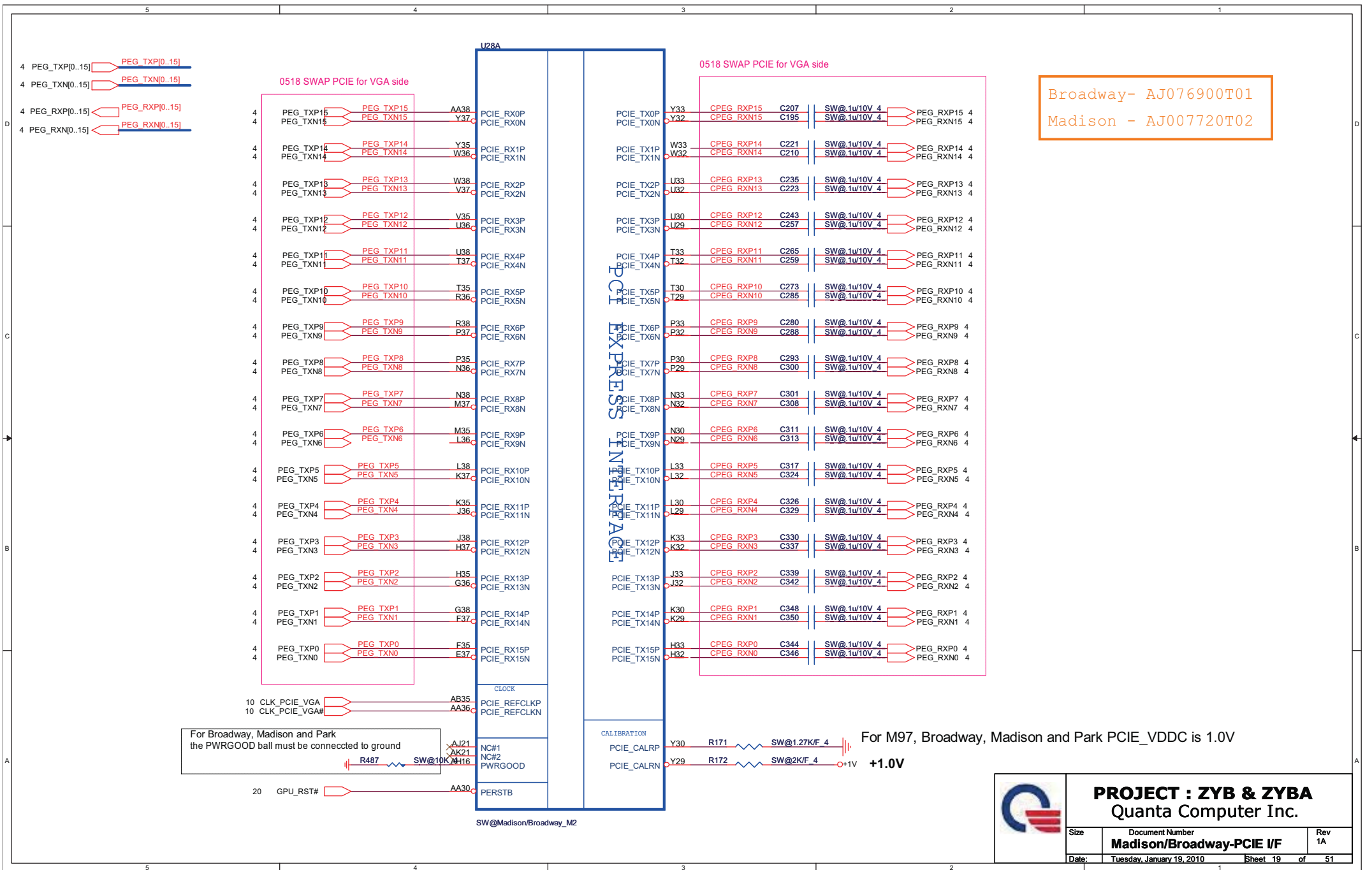


## Del Braidwood

18

### S3 leakage solution(CLG)



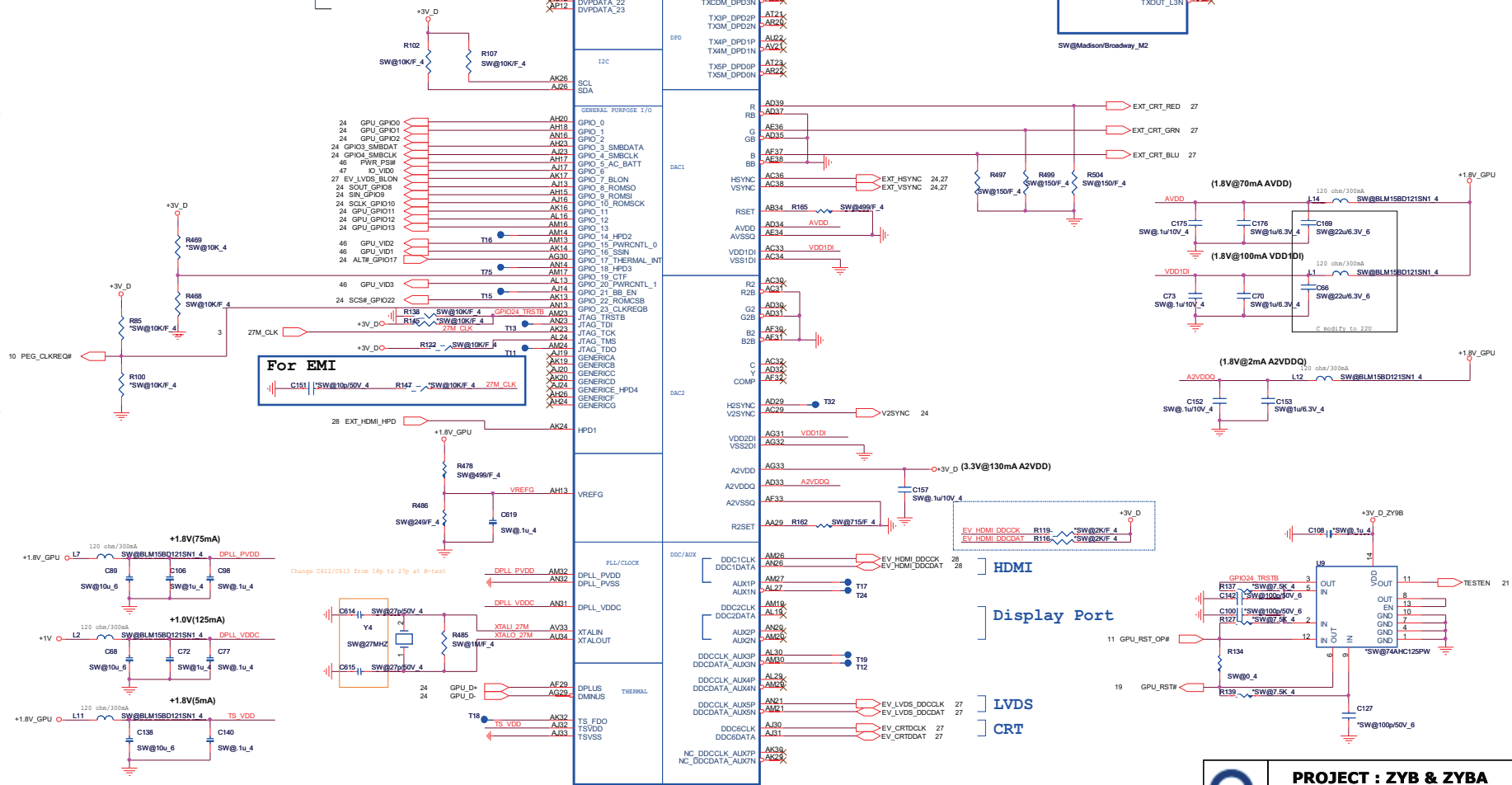


## GPU Power-on sequence

- 1 => +VGPU\_CORE
- 2 => +VGPU\_IO
- 3 => +1V
- 4 => +1.5V\_GPU
- 5 => +3V\_D
- 6 => +1.8V\_GPU
- 7 => dGPU\_PWROK

1.8V GPIO

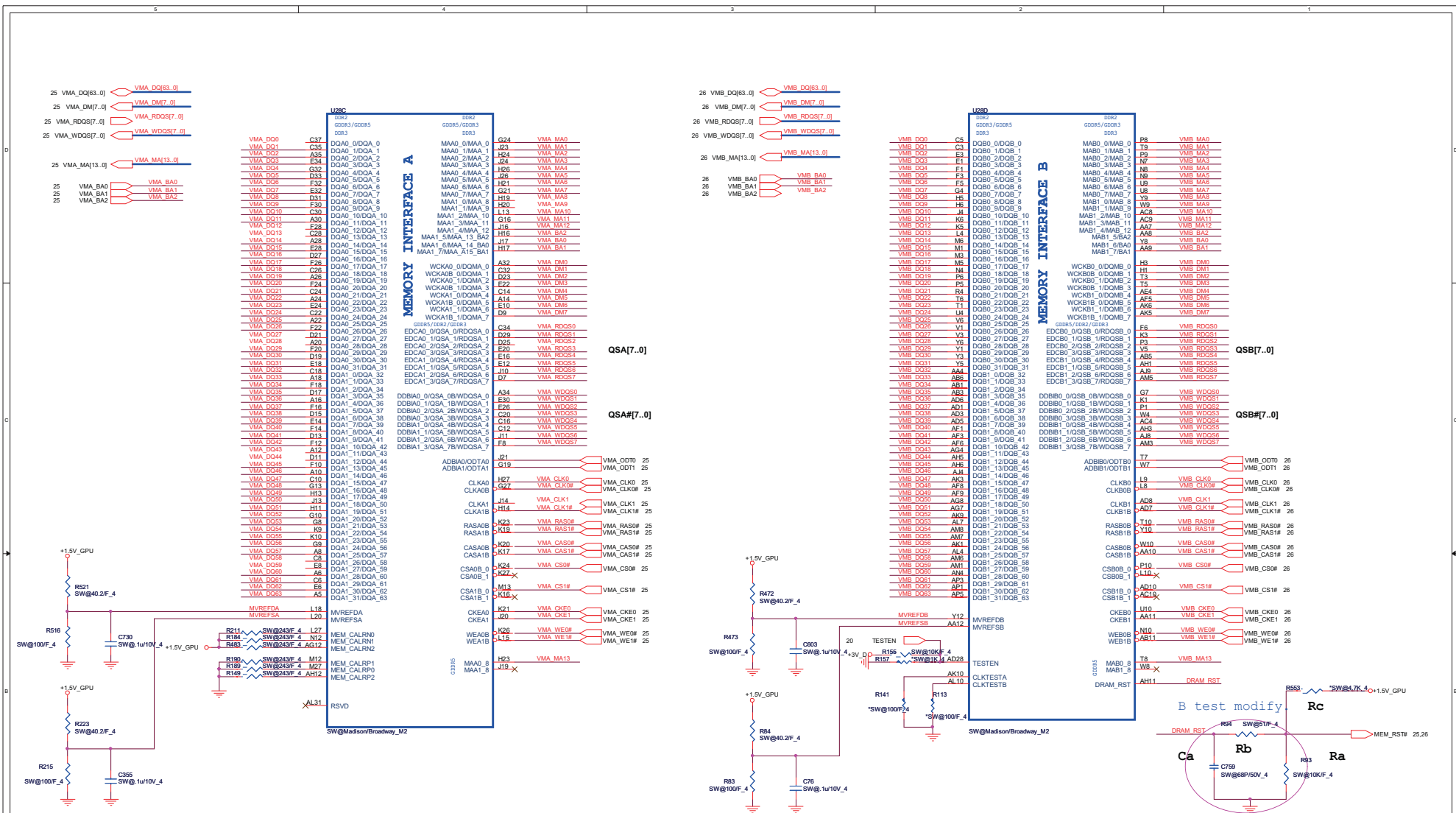
3.3V GPIO



**PROJECT : ZYB & ZYBA**  
**Quanta Computer Inc.**

Size: Document Number  
**Madison/Broadway-HOST I/F**  
Date: Tuesday, January 19, 2010 Sheet 20 of 51

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DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Designator	For M97-M2	For Mannhattan
Ra	10K	10K
Rb	0R/Short	51R
Rc	DNI	DNI
Ca	2.2nF	68pF

**PROJECT : ZYB & ZYBA**  
Quanta Computer Inc.

Size	Document Number	Rev
	Madison/Broadway-MEM I/F	1A
Date:	Tuesday, January 19, 2010	Sheet 21 of 51

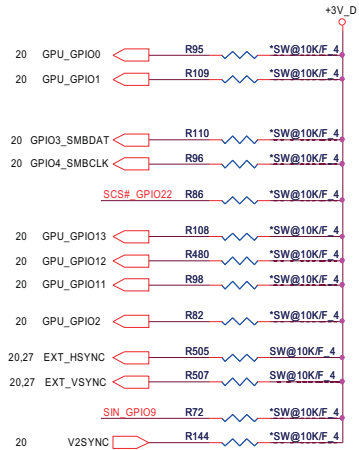








## PIN STRAPS



## Memory Aperture size

GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

## Audio Table

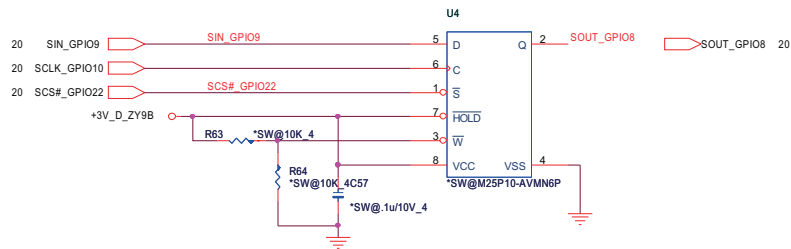
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by detect
1	0	DP only
1	1	Both DP & HDMI

## CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED ENABLE EXTERNAL BIOS ROM	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000	See Memory Aperture size
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[10] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

## EEPROM

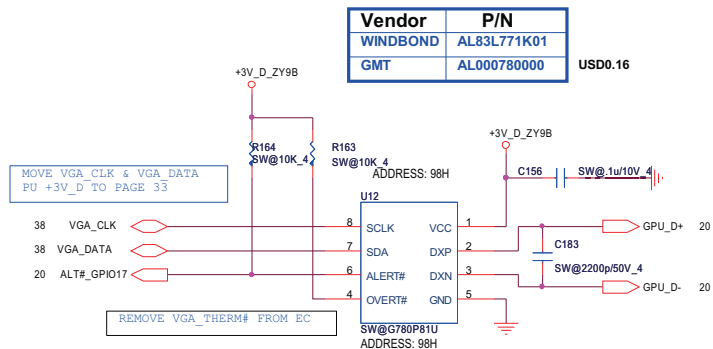


## DDR3 VRAM SIZE Strap

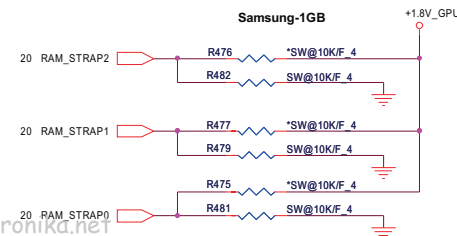
## DDR3 VRAM size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	512MB	1	1	0
			1GB	1	0	0
			2GB	1	0	1
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	512MB	0	1	0
			1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1
AMD	23EY2387MA-12	AKD5LGGT700		0	1	0

## Thermal Sensor



## Samsung-1GB

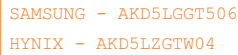


RAM\_STRAP2 SET DDR3 Vendor  
RAM\_STRAP[1:0] SET SIZE.

**PROJECT : ZYB & ZYBA**  
Quanta Computer Inc.

Size	Document Number	Rev
	Strip/Thermal	1A
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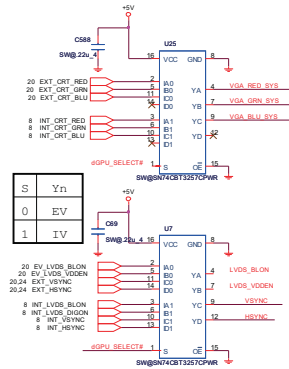




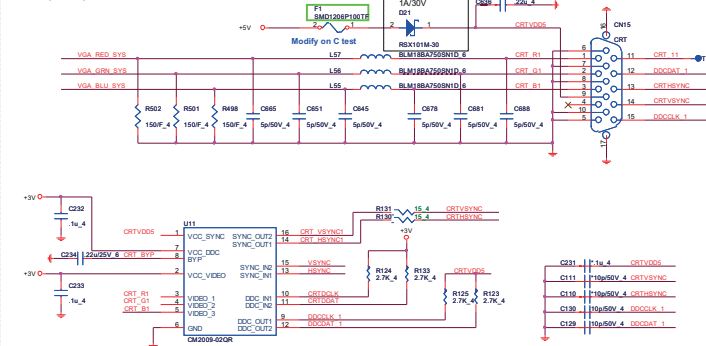
TOP Down



## CRT SWITCH(CRT)

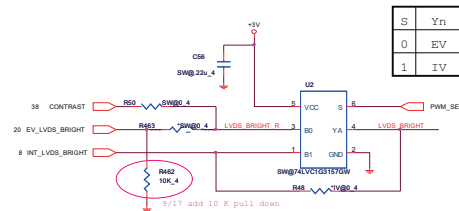


## CRT(CRT)

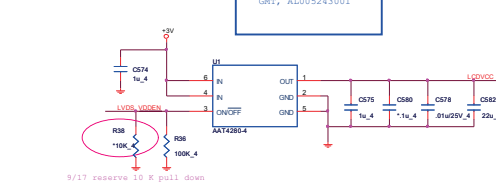


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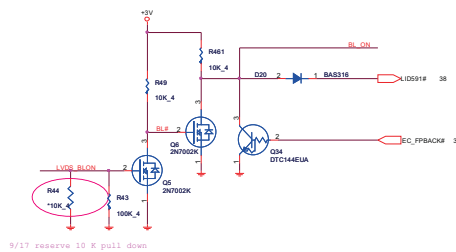
## LVDS(LDS)



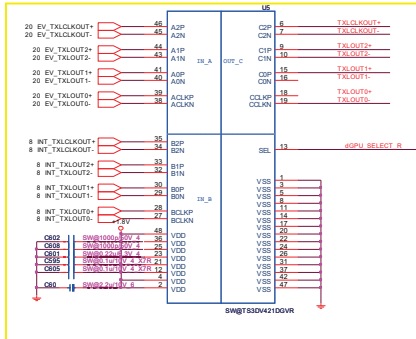
## LCD Power(LDS)



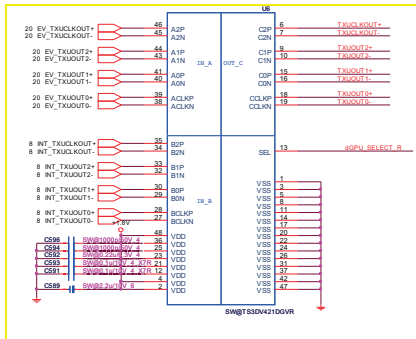
## Backlight Control(LDS)



### LVDS SW1



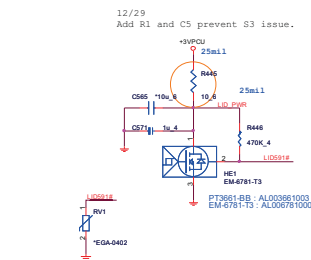
### LVDS SW2



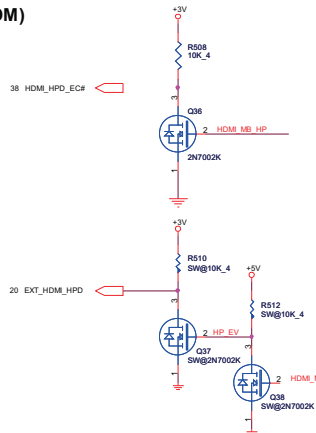
S	Yn
0	EV
1	IV

gGPU_SELECT#	Output
L	EV_LVDS
H	INT_LVDS

## Lid Switch (HSR)

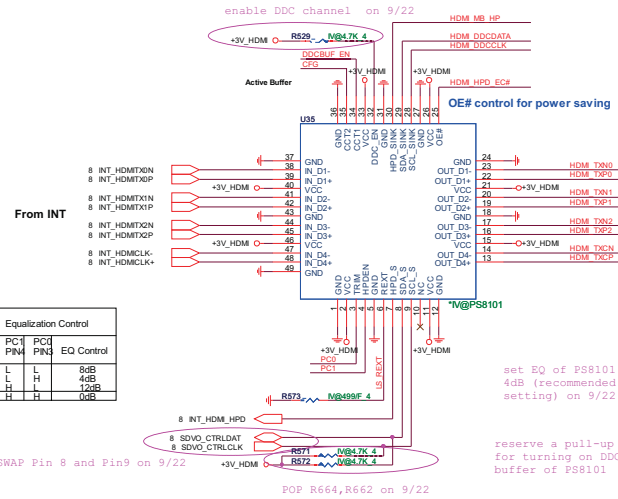


## HDMI HPD(HDM)



## HDMI LEVEL SHIFTER(HDM)

PS8101 :: AL008101000

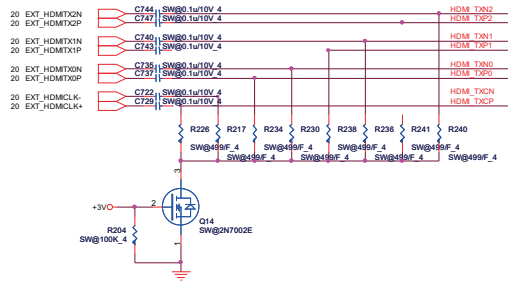


UMA => PS8101 Exist  
SG and Dis only => PS8101 del

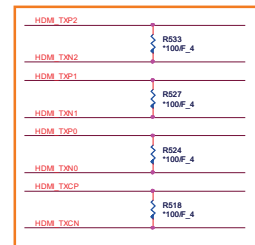
28

## (HDM)

### From EXT VGA

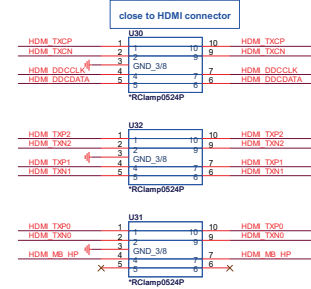


## EMI reserve for HDMI(HDM)

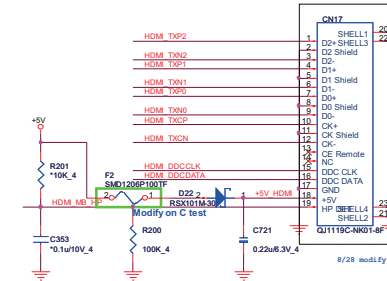


Close connector

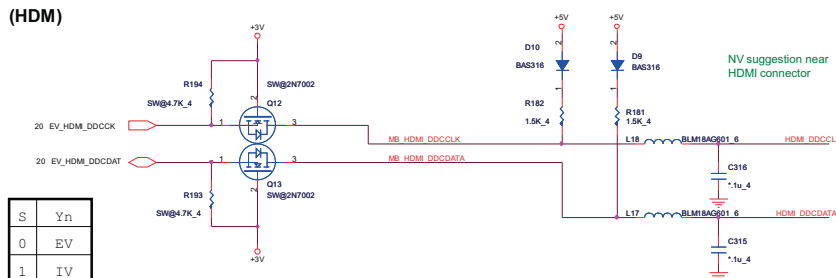
## ESD Protect



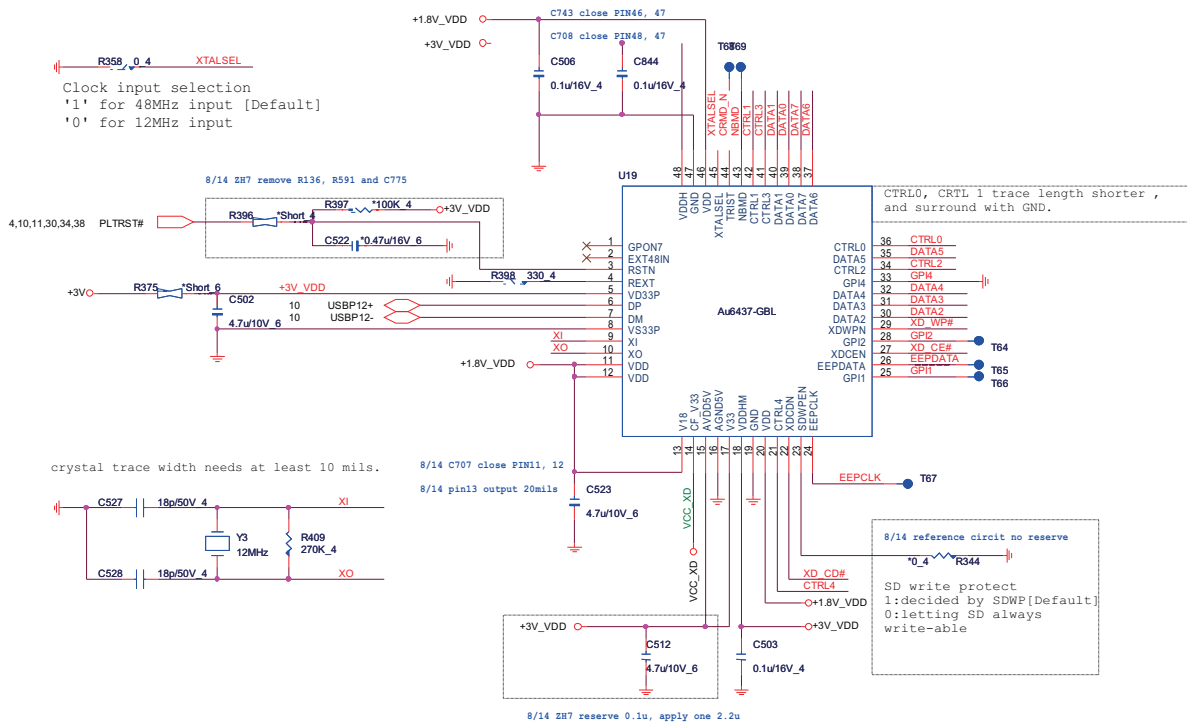
## HDMI connector(HDM)



## (HDM)

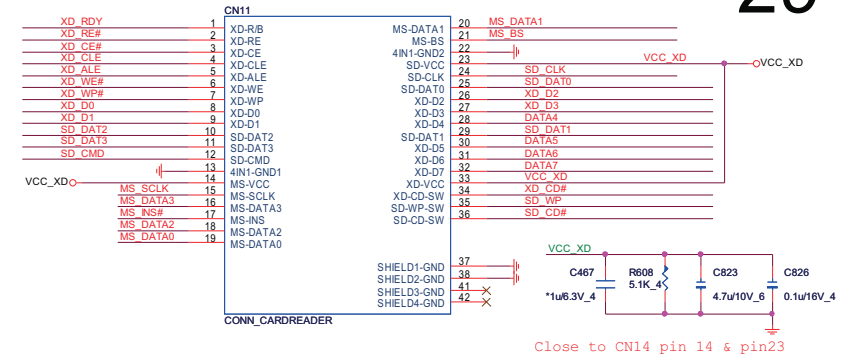


### AU6433 CardReader(MMC)

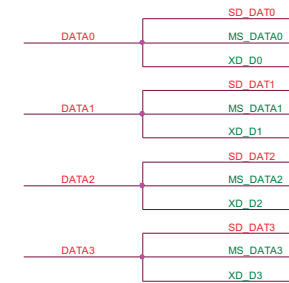


## 4 IN 1 CARD READER (MMC)

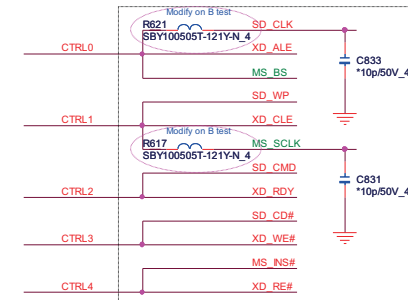
29



Main	DFHD36MS017
Second	DFHD38MS013



Close to connector

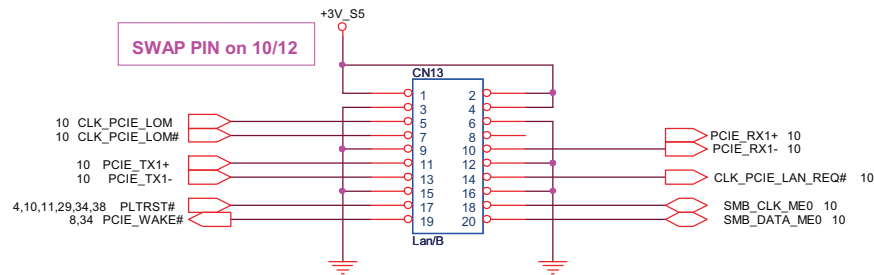


**PROJECT : ZYB & ZYBA**  
Quanta Computer Inc.

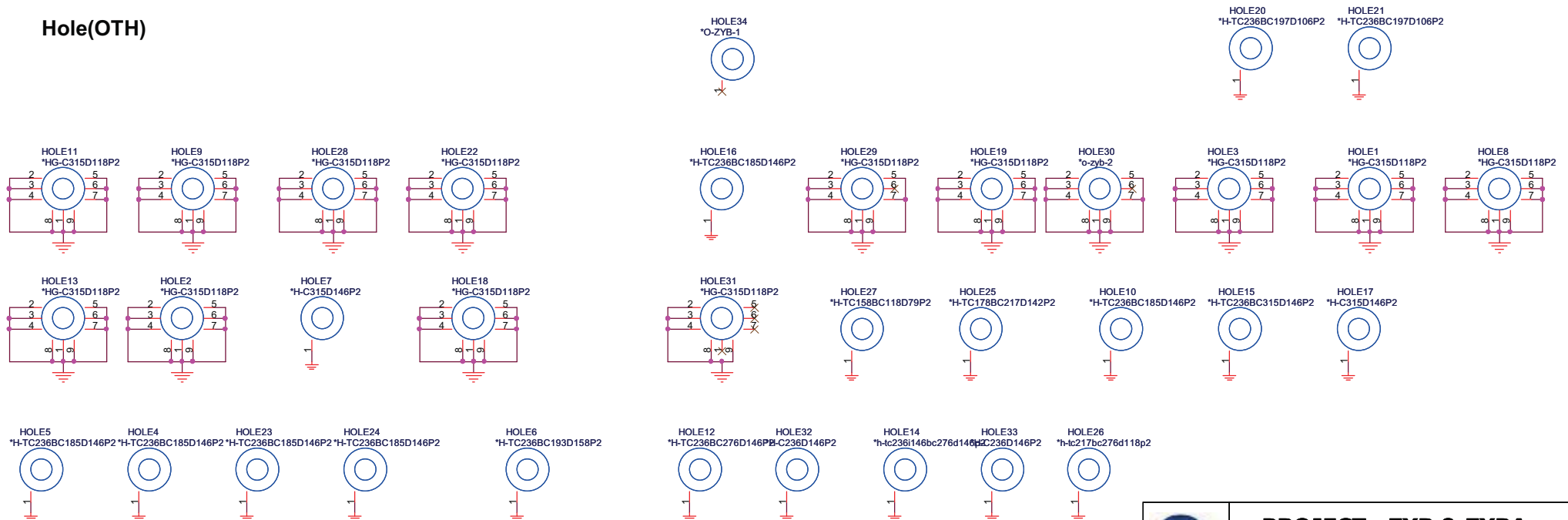
Size	Document Number <b>AU6433 CardReader</b>	Rev 1A
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## Lan/B(LAN)



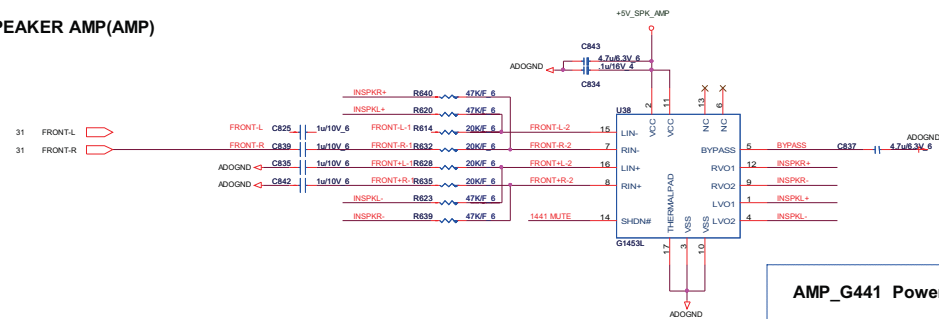
## Hole(OTH)



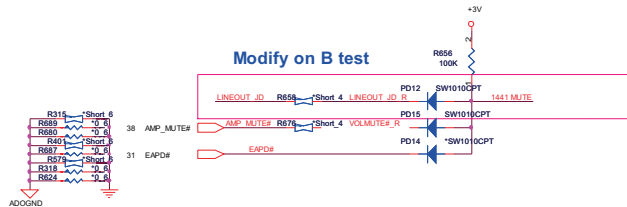
 <b>PROJECT : ZYB &amp; ZYBA</b> <b>Quanta Computer Inc.</b>		
Size	Document Number	Rev
	<b>Lan/B &amp; Hole</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 30 of 51



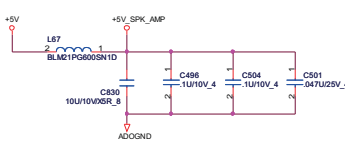
## SPEAKER AMP(AMP)



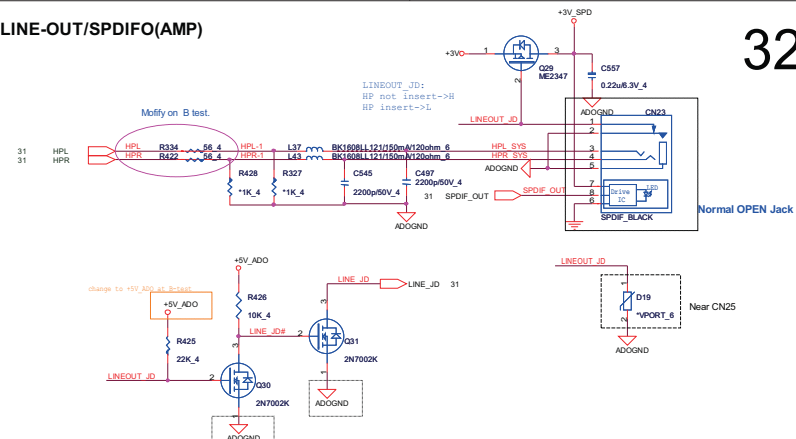
### Modify on B test



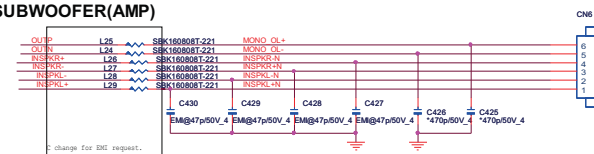
## AMP\_G441 Power(ADO)



## LINE-OUT/SPDIFO(AMP)



## Main SPK and SUBWOOFER(AMP)

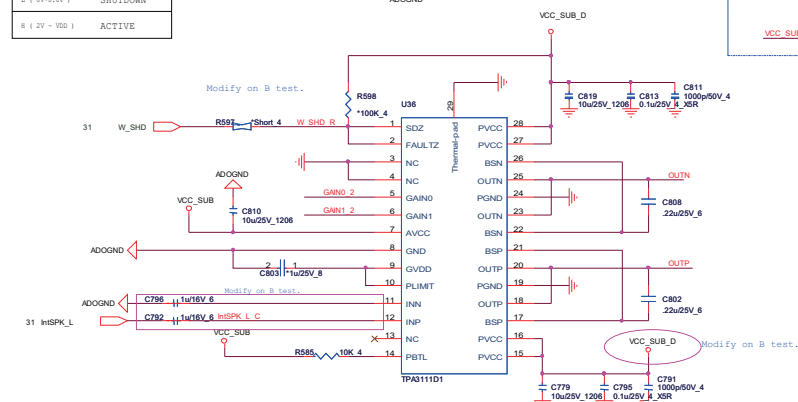


## SUBWOOFER(AMP)

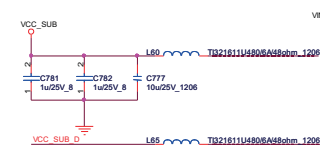
LFF for  $f_c(-3dB)=500Hz$

SD : shutdown signal for IC10M=disable , HSD=enable

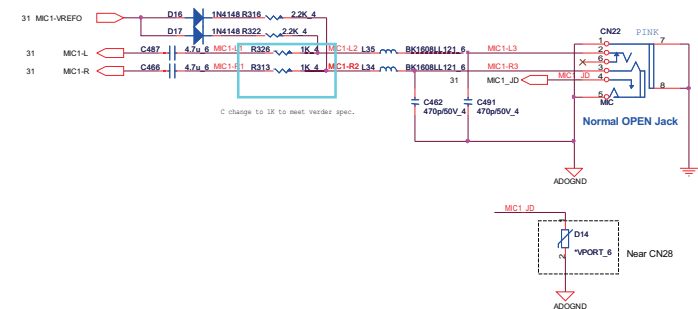
SHUTDOWN	TPA3110D1
1 ( 0V-0.8V )	SHUTDOWN
8 ( 2V - 5V )	ACTIVE



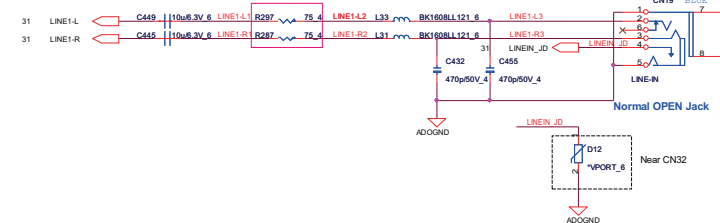
## SUBWOOFER Power(AMP)



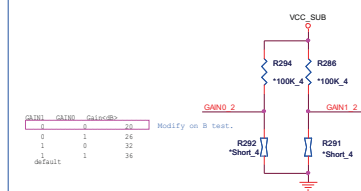
## MIC(AMP)



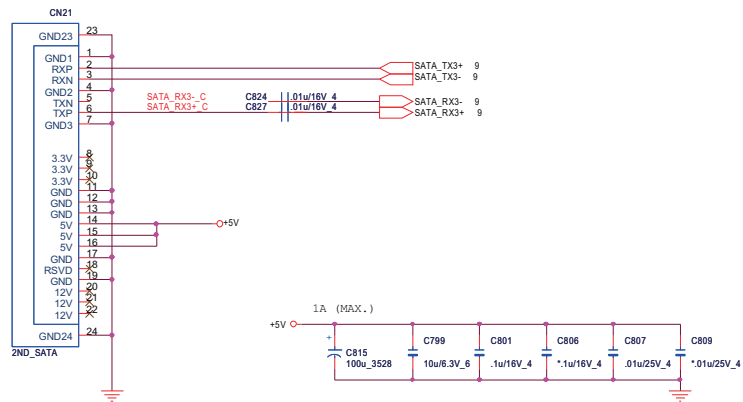
## LINE IN(AMP)



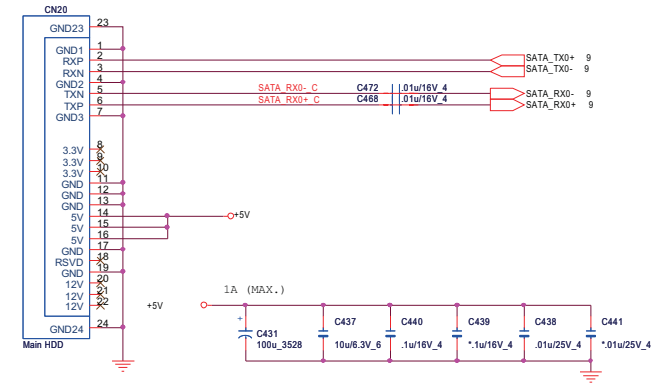
## AMO GAIN(AMP)



## 2nd SATA HDD (HDD)

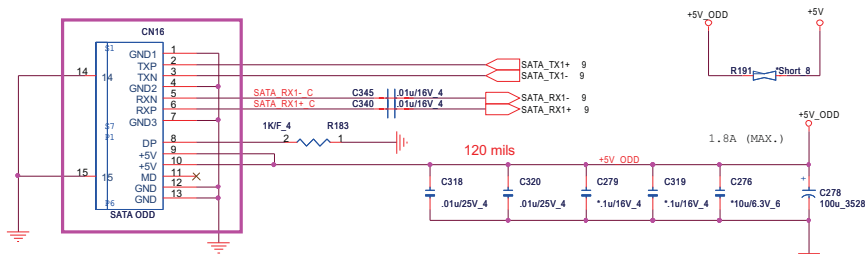


## MAIN SATA HDD(HDD)



## ODD SATA(ODD)

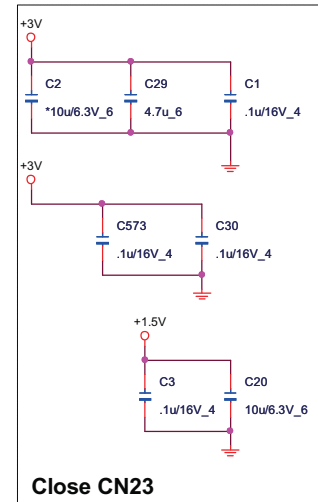
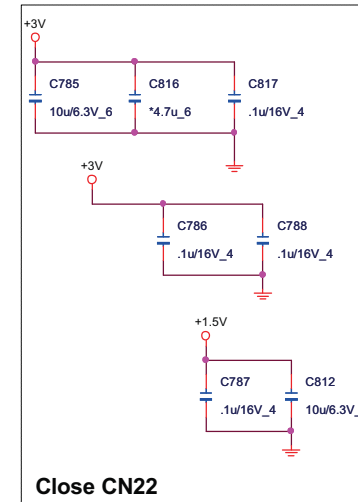
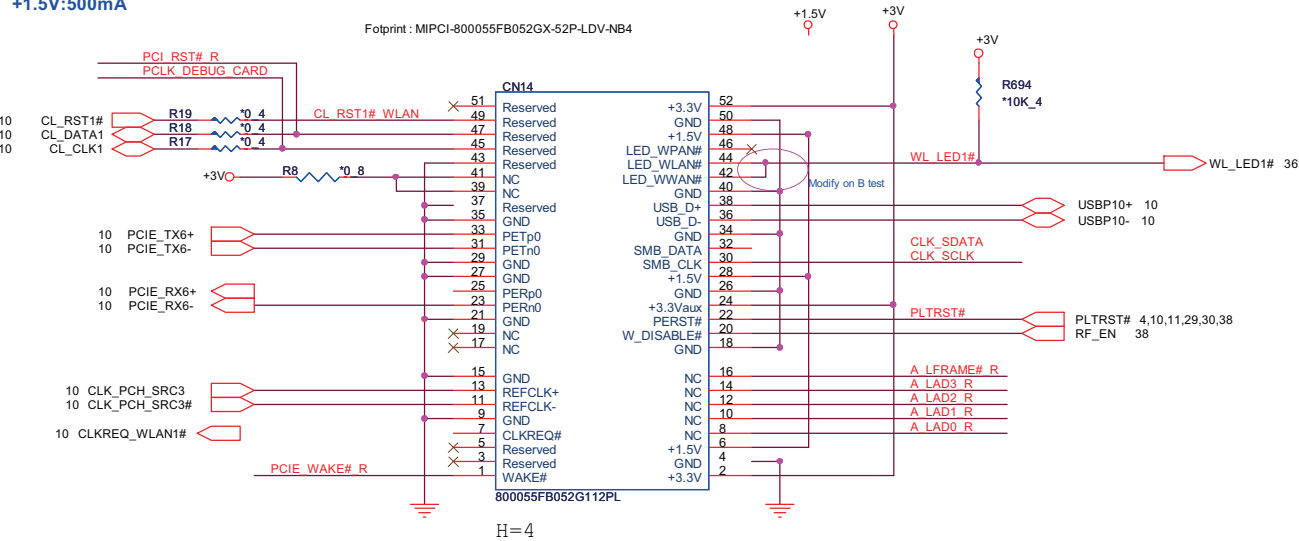
This ODD must be use eSATA Port



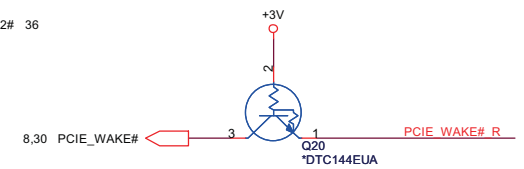
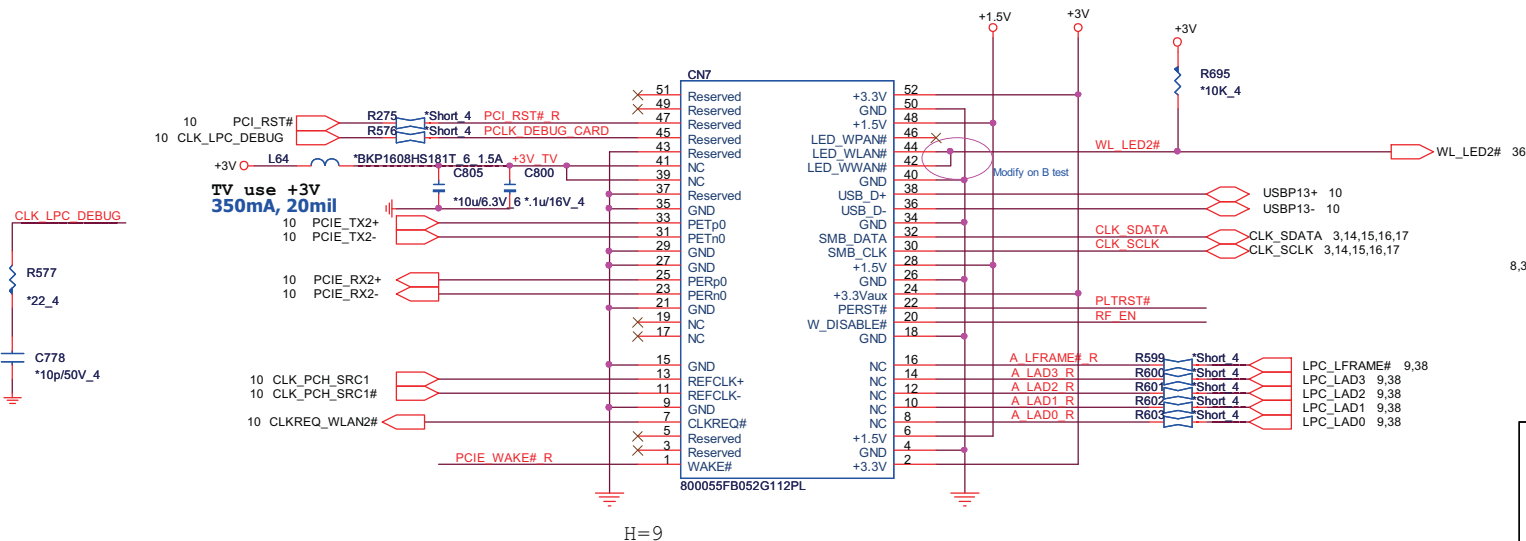
## Wireless 1(MPC)


+3.3V: 1000mA  
+3.3Vaux: 330mA  
+1.5V: 500mA

Fotprint : MIPCI-800055FB052GX-52P-LDV-NB4

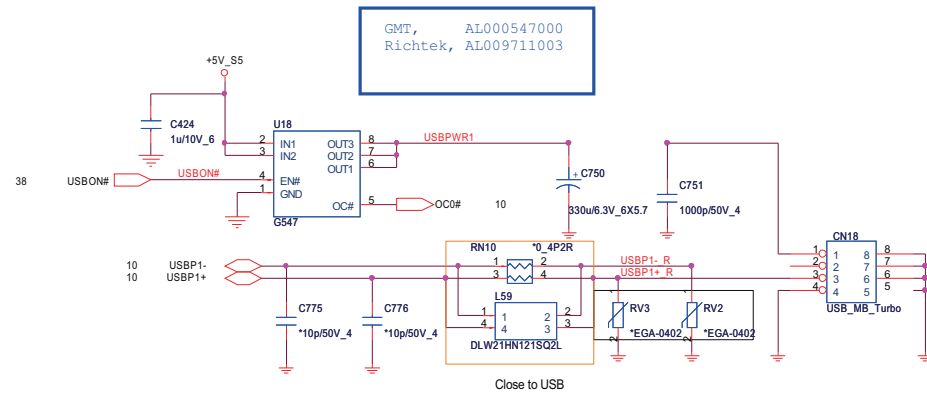


## Wireless 2 (MPC)

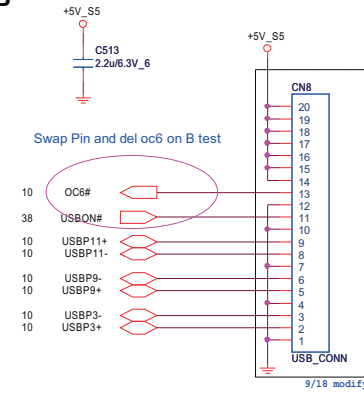


 <b>PROJECT : ZYB &amp; ZYBA</b> Quanta Computer Inc.		
Size	Document Number	Rev
	<b>MINI PCI-E card</b>	<b>1A</b>
Date:	Tuesday, January 19, 2010	Sheet 34 of 51

## USB(USB)



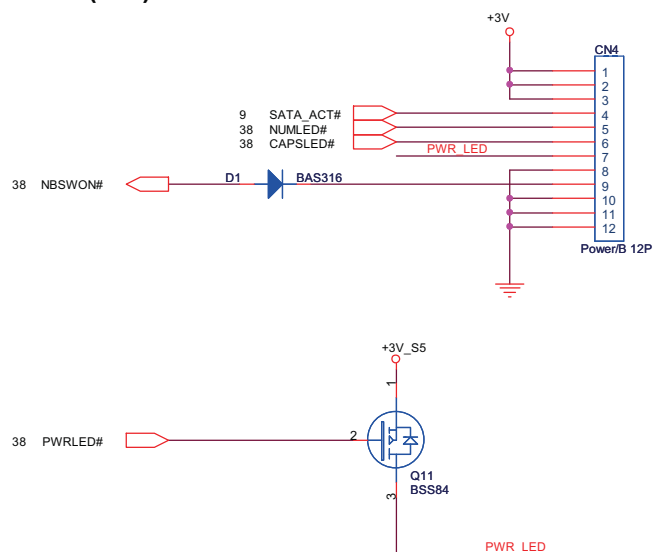
## USB/B



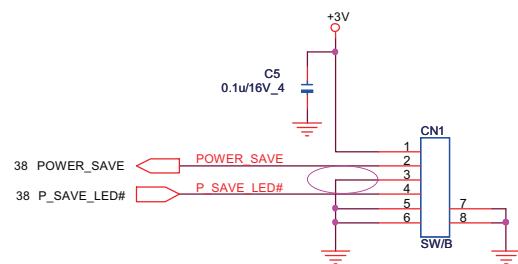
35



## POWER BOARD(UIF)

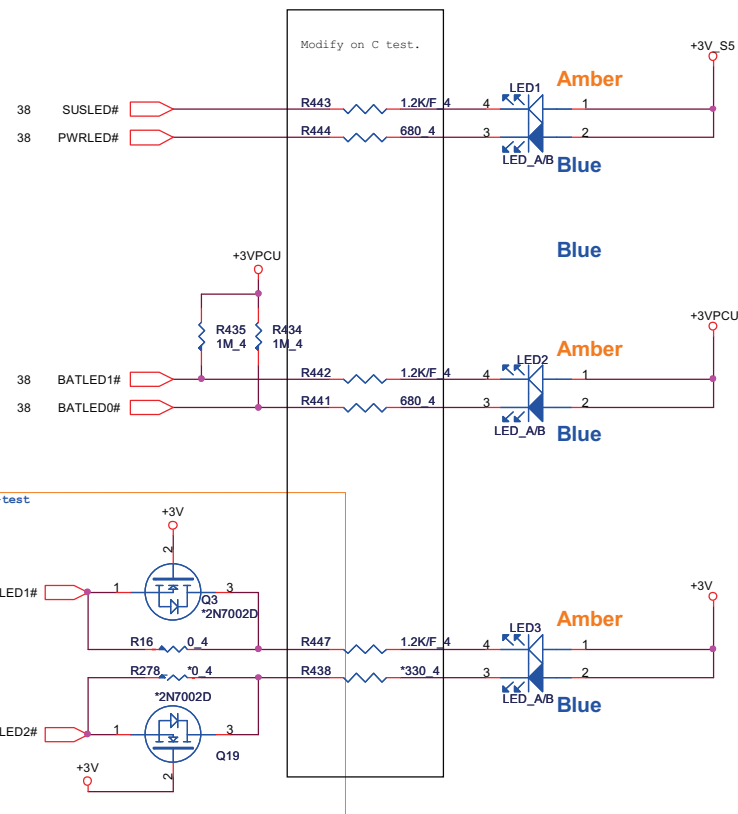



## SW/B(UIF)



## M/B(Battery) LED(uif)

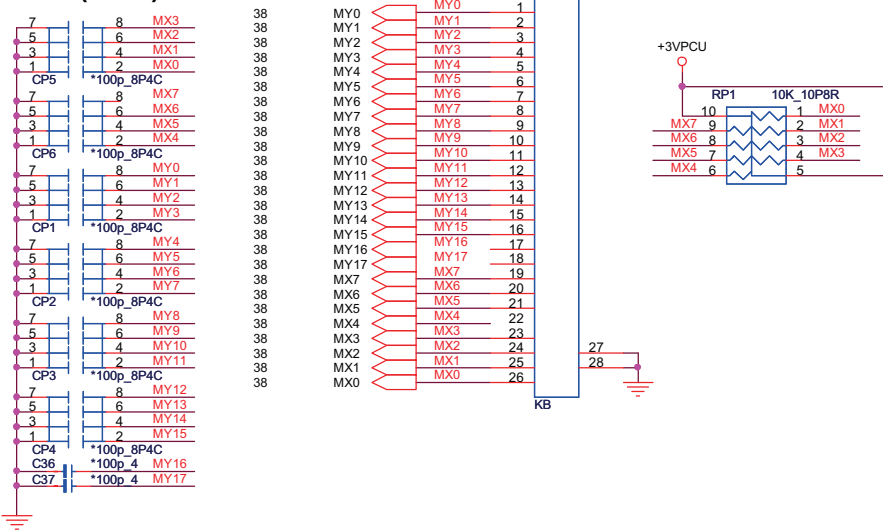
36



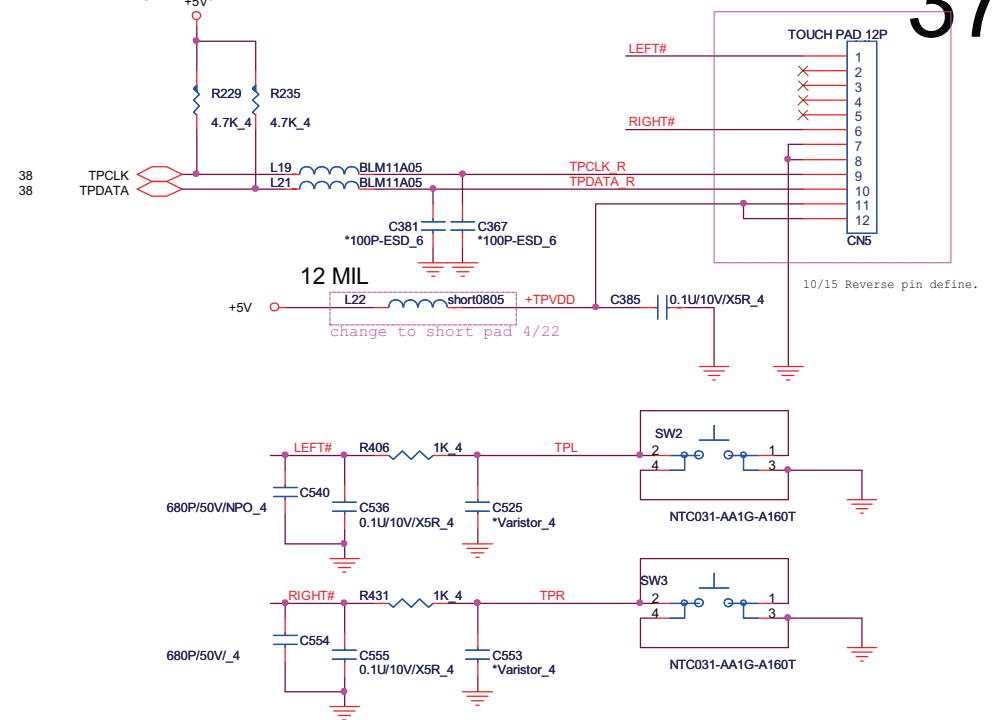
 <b>PROJECT : ZYB &amp; ZYBA</b> Quanta Computer Inc.		
Size	Document Number	Rev
	<b>POWER/LAUNCH/LED</b>	1A
Date:	Tuesday, January 19, 2010	Sheet 36 of 51



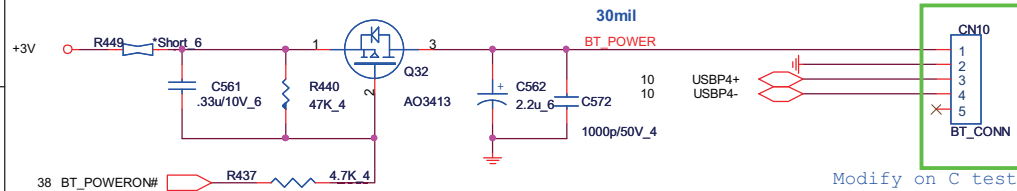
## INT K/B(KBC)



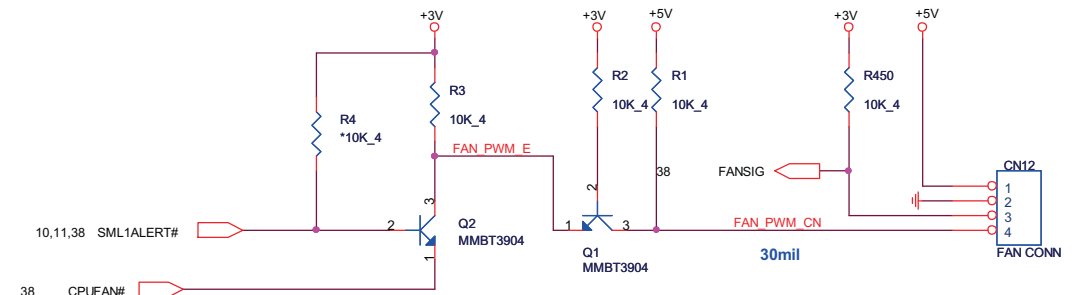
## TOUCHPAD(TPD)



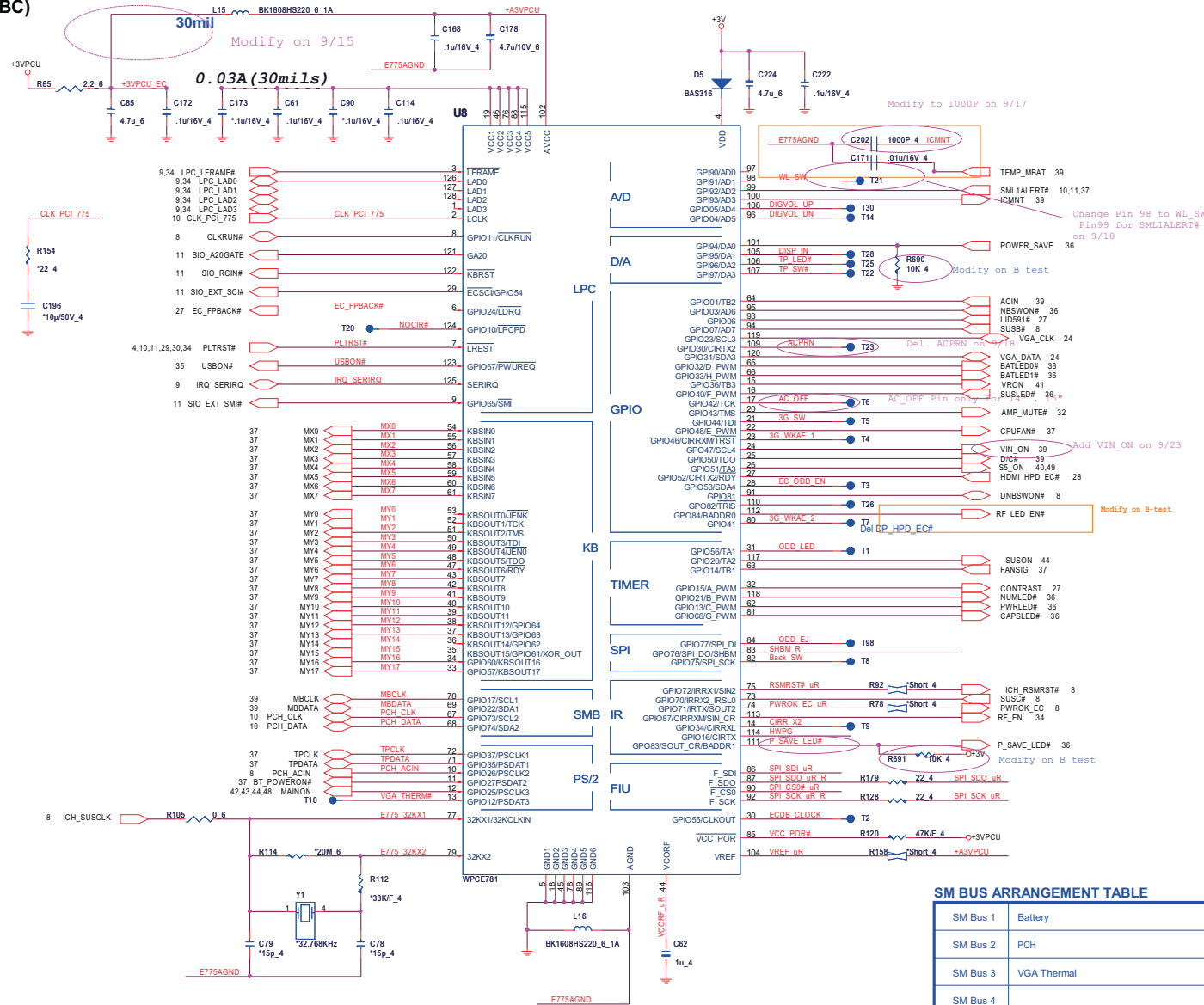
## BLUETOOTH CONNECTOR(BTM)



## CPU FAN(THM)



## EC(KBC)



## I/O ADDRESS SETTING

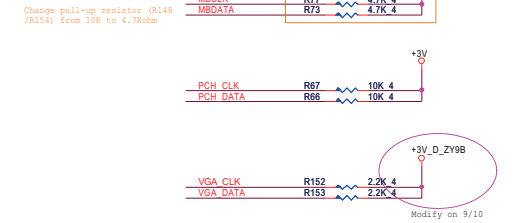
38

SHBM=0: Enable shared memory with host BIOS

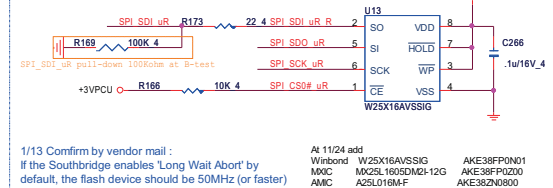
SHBM R R118 10K 4

1/13 Confirm by vendor mail :  
Disabled (\*) if using FW device on LPC.  
Enabled (0) if using SPI flash for both system BIOS and EC firmware

## SM BUS PU



## SPI FLASH

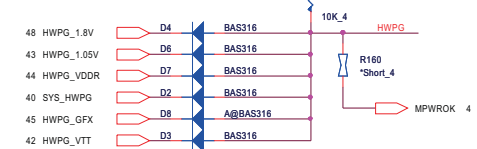


1/13 Confirm by vendor mail :  
If the Southbridge enables Long Wait Abort by default, the flash device should be 50MHz (or faster)

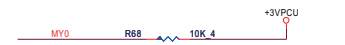
At 11/24 add:  
Winbond W25X16AVSSIG  
MXC MX25L1605DM21-12G  
AMC A25L016M-F

AKE38FP0N01  
AKE38FP0Z00  
AKE38ZNR000

## HWPG

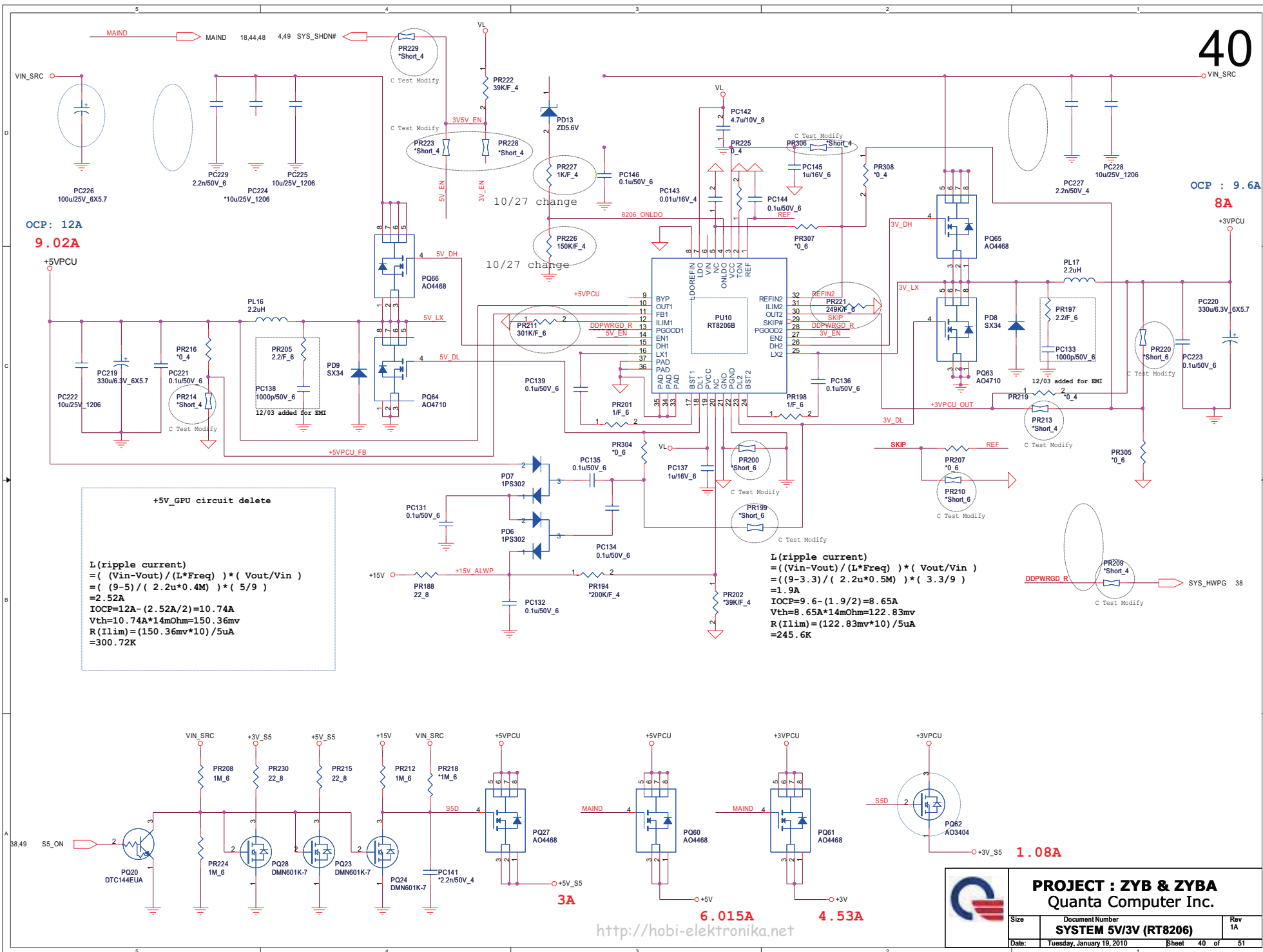


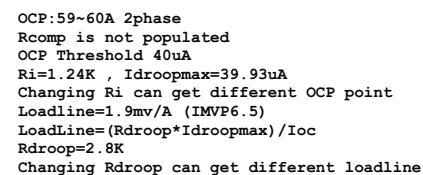
## INTERNAL KEYBOARD STRIP SET



		<b>PROJECT : ZYB &amp; ZYBA</b> <b>Quanta Computer Inc.</b>	
		<b>WPCE81 &amp; FLASH</b>	<b>Rev 1A</b>
<b>Date:</b> Tuesday, January 19, 2010	<b>Document Number:</b>	<b>Sheet:</b> 38	<b>of:</b> 51



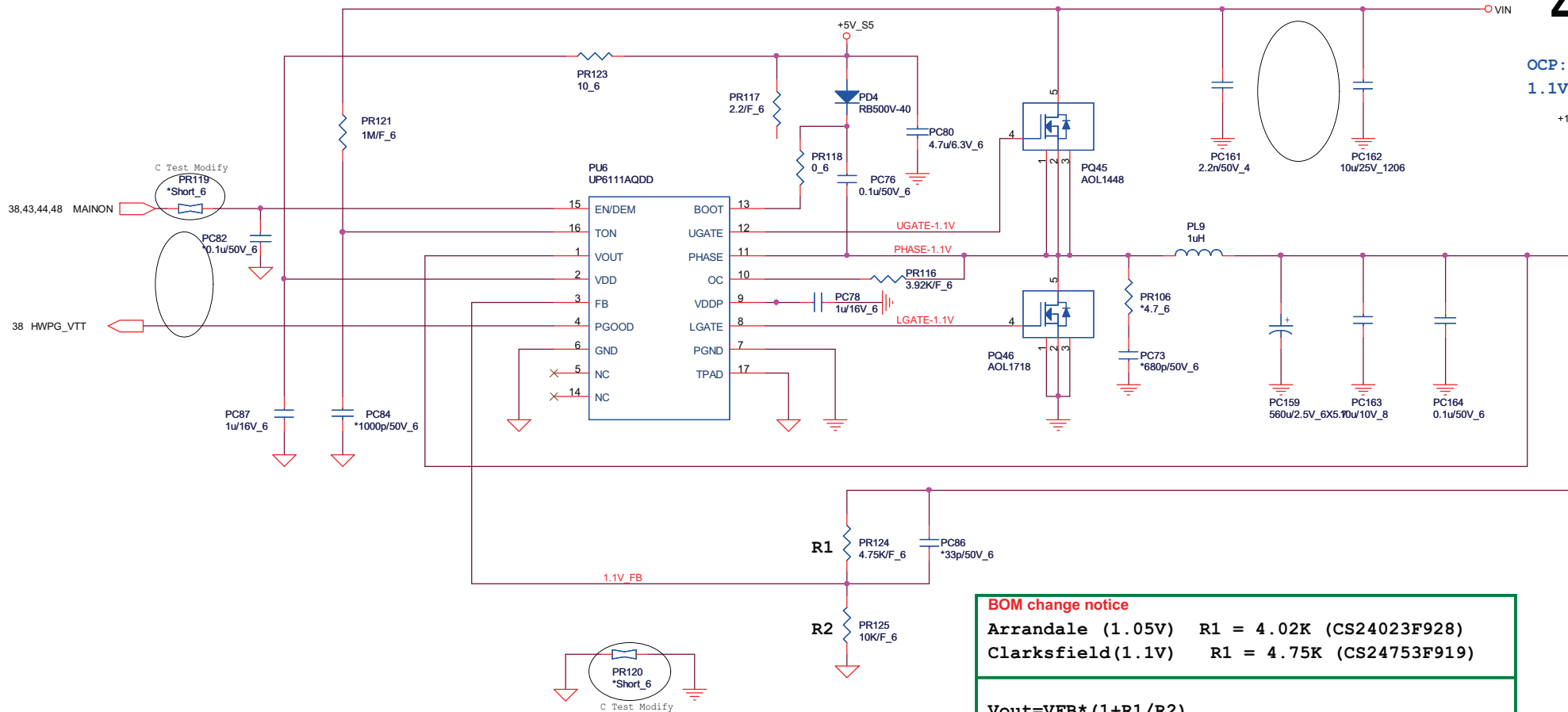




[ PWM ]

42

OCP: 18A  
1.1V/13.5A



**BOM change notice**

Arrandale (1.05V) R1 = 4.02K (CS24023F928)  
 Clarksfield(1.1V) R1 = 4.75K (CS24753F919)

$V_{out} = V_{FB} * (1 + R1/R2)$   
 $V_{FB} = 0.75V$

$TON = 3.85p * RTON * V_{out} / (V_{in} - 0.5)$

$Frequency = V_{out} / (V_{in} * TON)$


$TON = 3.85p * 1M * 1 / (V_{in} - 0.5)$

$Frequency = 1 / (0.0036767) = 272K$

AO1718  $R_{dson} = 3 \sim 4.3m\Omega$

$L(ripple\ current)$   
 $= (19 - 1.1) * 1.1 (1u * 272k * 19)$   
 $\sim 3.81A$

$4.3m * 18 = RILIM * 20uA$   
 $RILIM = 3.87K \text{ --- } 3.92K$

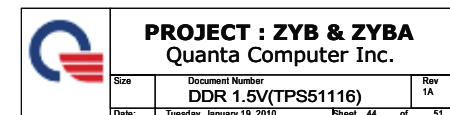
 <b>PROJECT : ZYB &amp; ZYBA</b> Quanta Computer Inc.		
Size	Document Number +VTT (UP6111A)	Rev 1A
Date:	Tuesday, January 19, 2010	Sheet 42 of 51



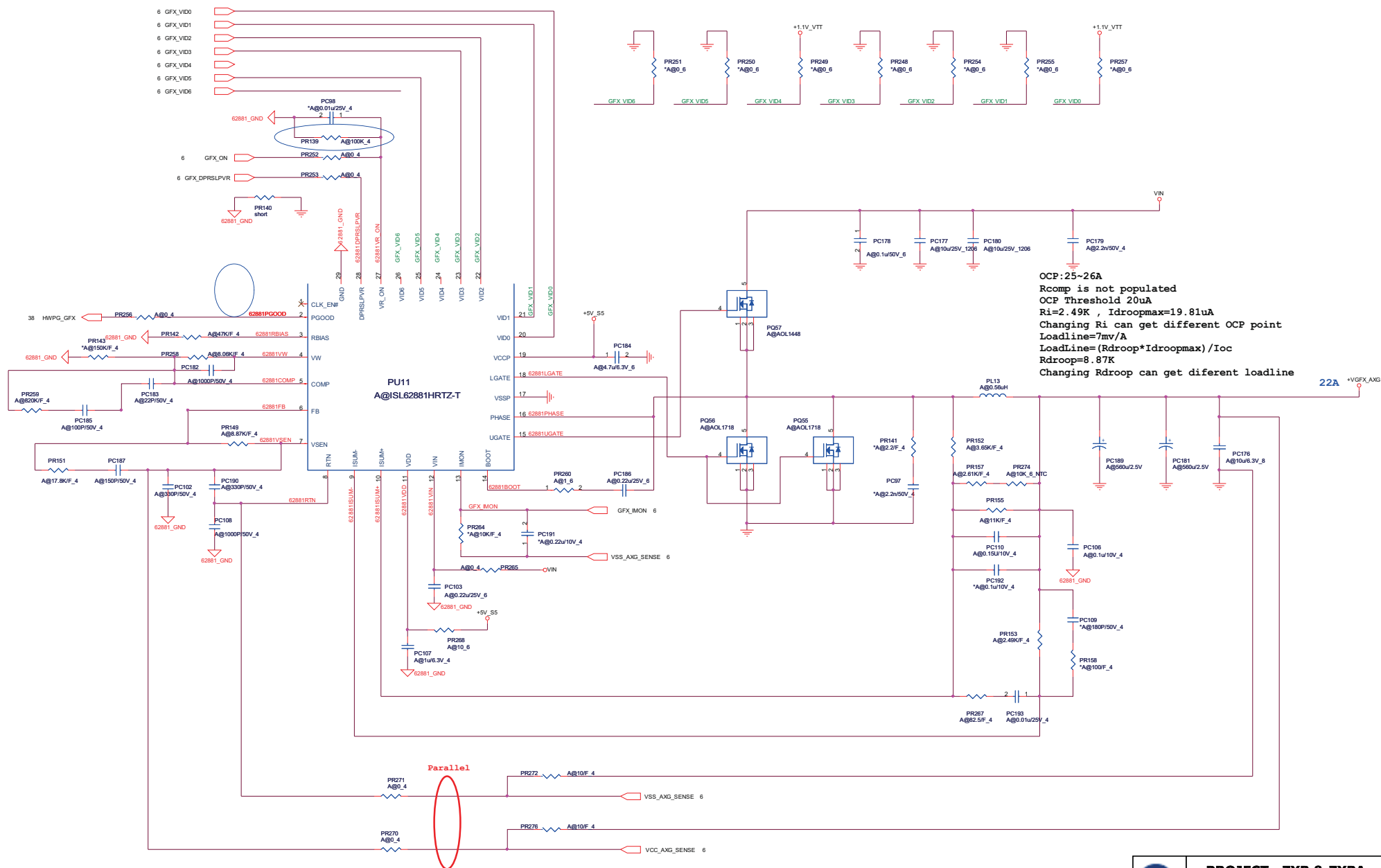


**PROJECT : ZYB & ZYBA**  
Quanta Computer Inc.

Size	Document Number <b>VCCP +1.05V (UP6111A)</b>	Rev 1A
Date:	Tuesday, January 19, 2010	Sheet 43 of 51



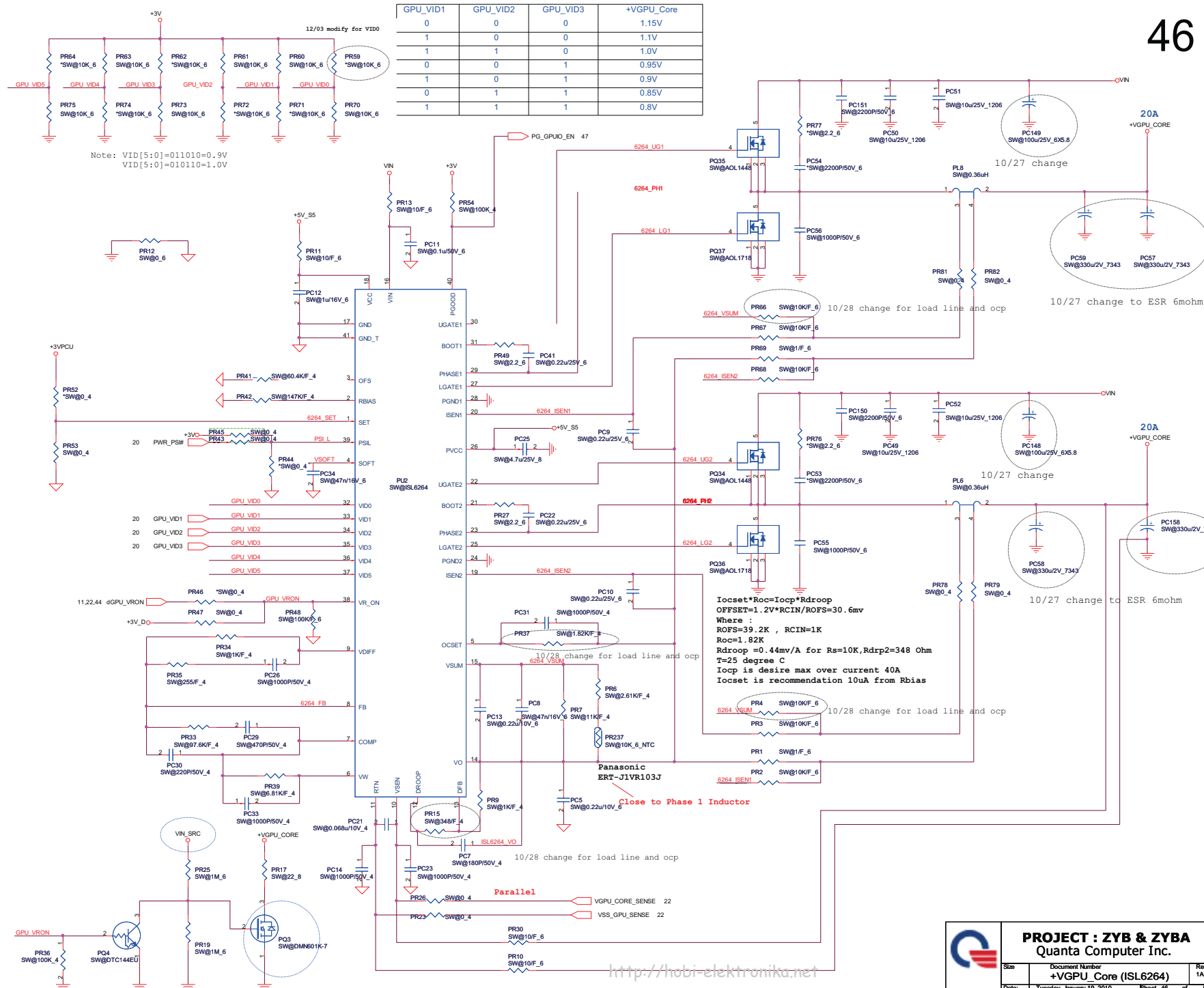
UMA &SG => +VGFX\_AXG Exist  
Discrete =>+VGFX AXG del



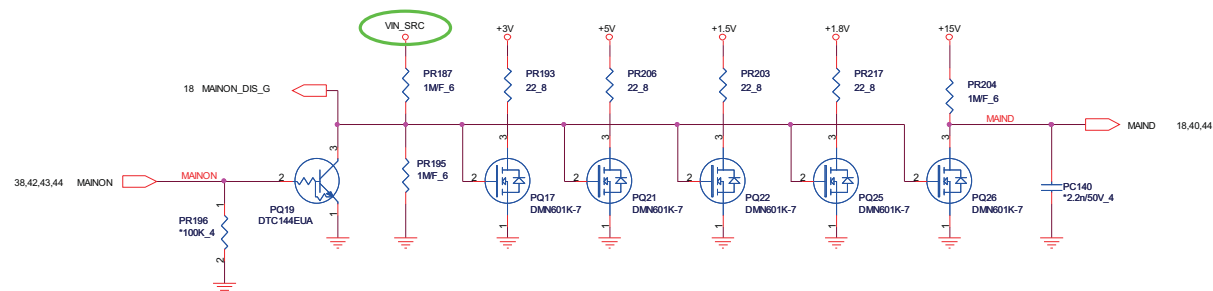
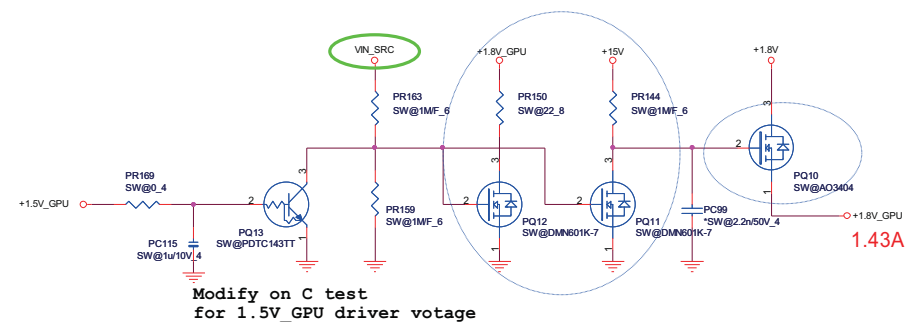
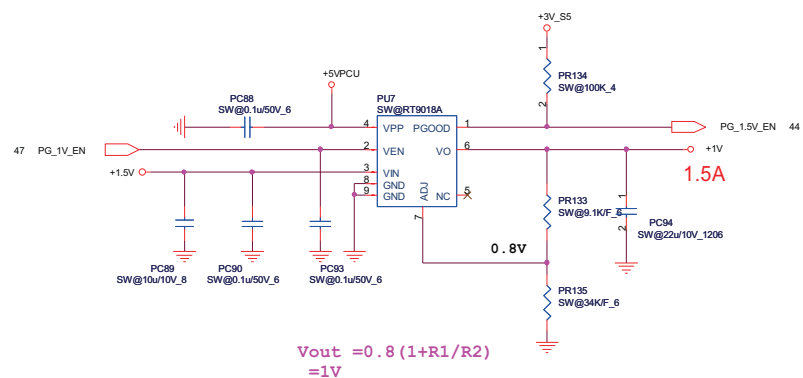
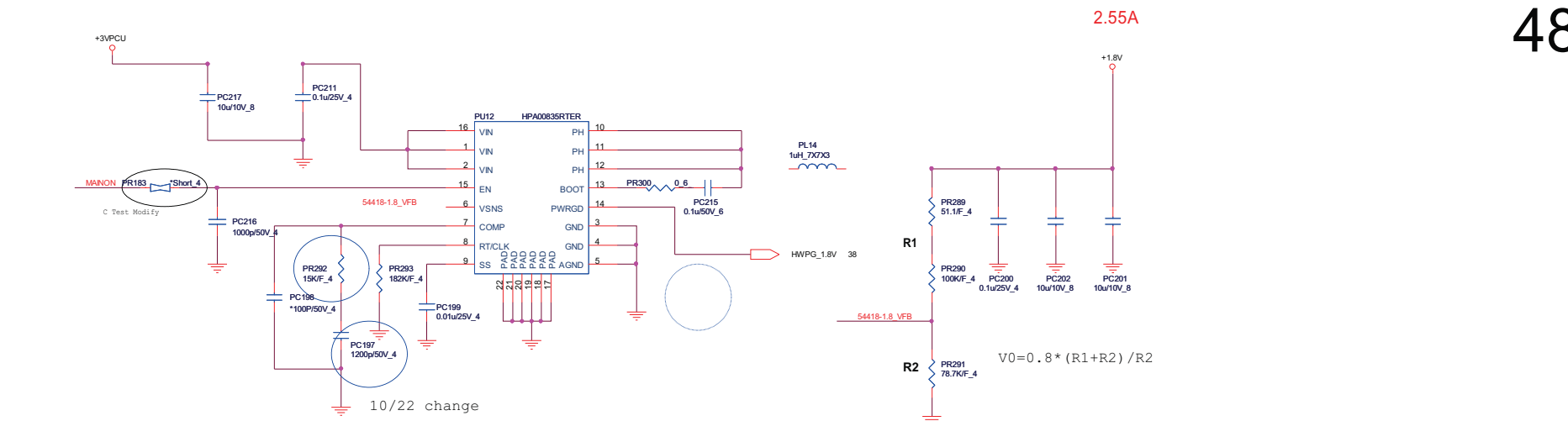
```
OCP:25~26A
Rcomp is not populated
OCP Threshold 20uA
Ri=2.49K , Idroopmax=19.81uA
Changing Ri can get different OCP point
LoadLine=7mv/A
LoadLine=(Rdroop*Idroopmax)/Ioc
Rdroop=8.87K
Changing Rdroop can get different loadline
```

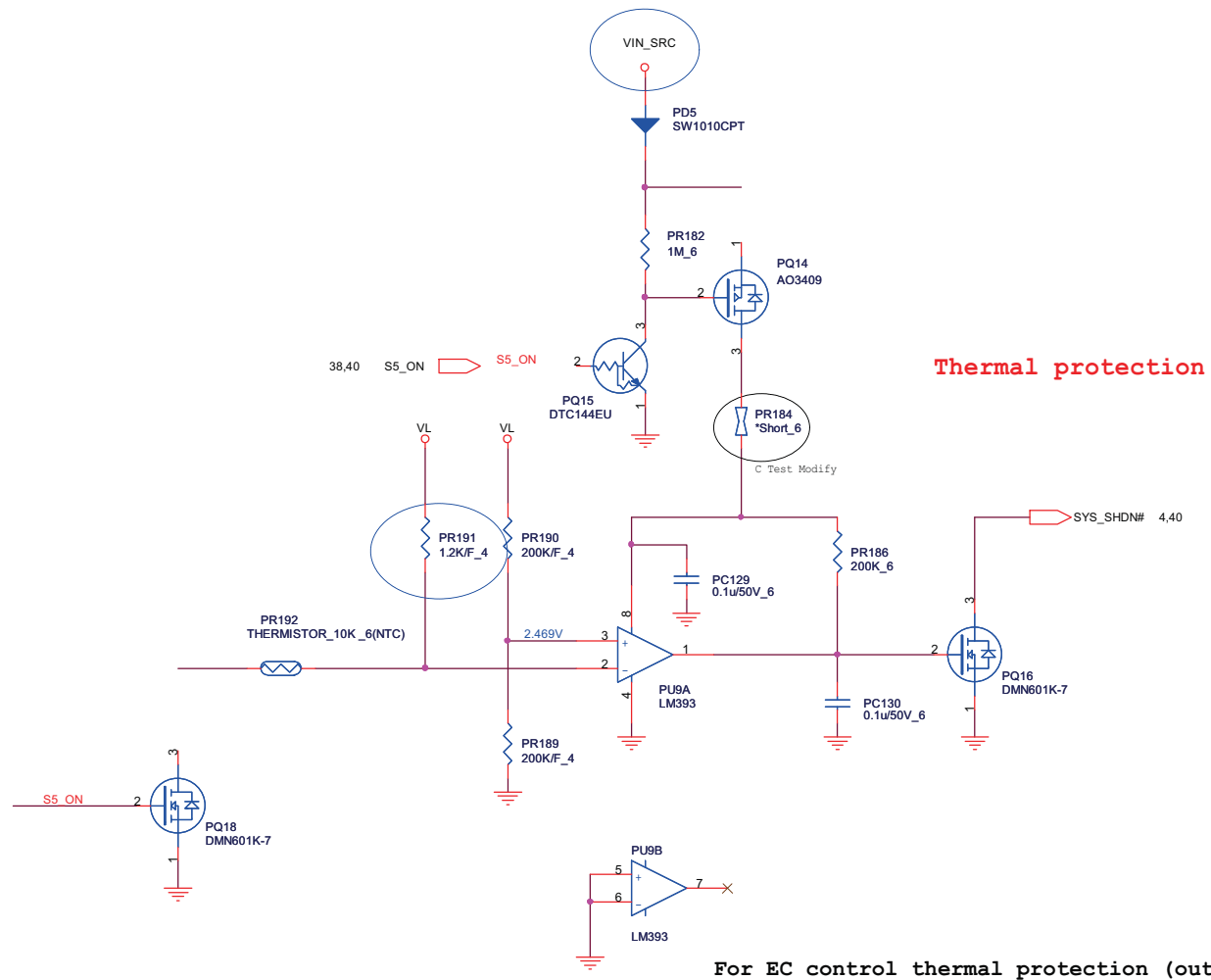
22A +VGFX\_AXG


2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.









 <b>PROJECT : ZYB &amp; ZYBA</b> Quanta Computer Inc.		
Size	Document Number	Rev
	<b>Thermal protect</b>	1A
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[illegible]

[illegible]